Brock J. LaMeres

Agilent Technologies

“RF Effects in PCB Design”

April 2001

Topics:

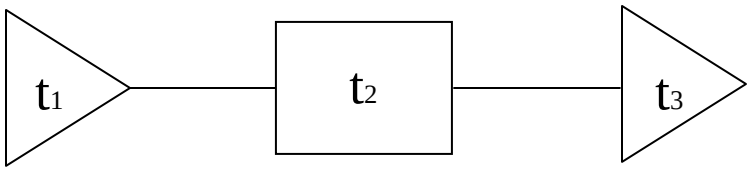
1) **Printed Circuit Board Via**

2) **Bandwidth Estimation**

3) **Effect of Via on Bandwidth**

PCB Bandwidth Estimation
(Background)

- **The overall risetime of a system is the RMS average of all risetimes in the system:**



$$t_{system} = \sqrt{t_1^2 + t_2^2 + t_3^2}$$

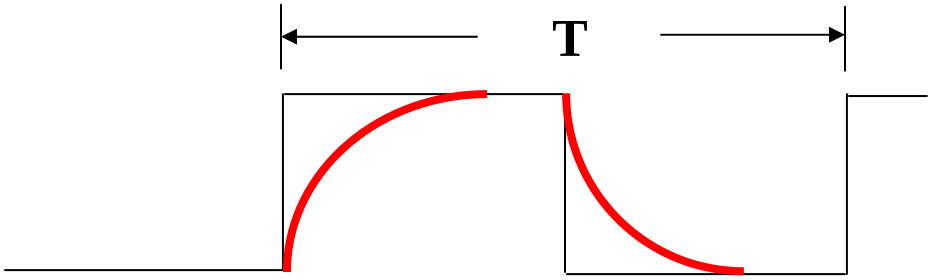
Risetime to Bandwidth Conversion
(Risetime BW Product)

$$t_{RISE} * BW = 0.35$$

PCB Bandwidth Estimation
(Background)

- **The MAXIMUM Toggle rate of a digital system is:**

$$f_{\max} = \frac{0.35}{t_{RISE}}$$



Time Constant to Risetime Conversion

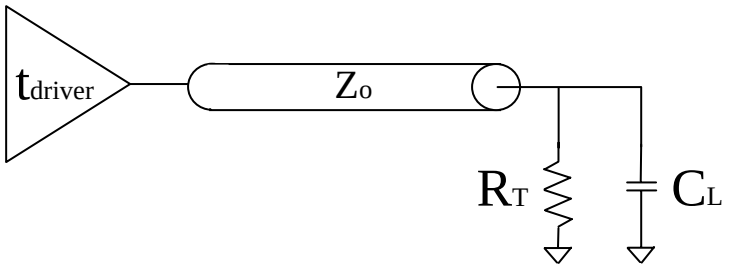
$$t_{RISE} = 2.2 * Tau$$

(Tau = RC or ZC)

PCB Bandwidth Estimation
(Series vs. Parallel Termination)

Parallel Termination Example

t_{driver} = 400 ps
$Z_o = R_L = 50\ \Omega$
C_L=6 pF



$Tau(\text{load}) = (50//50)*6p$ = 150 ps

$t_{rise}(\text{load}) = 2.2*(150p)$ = 330 ps

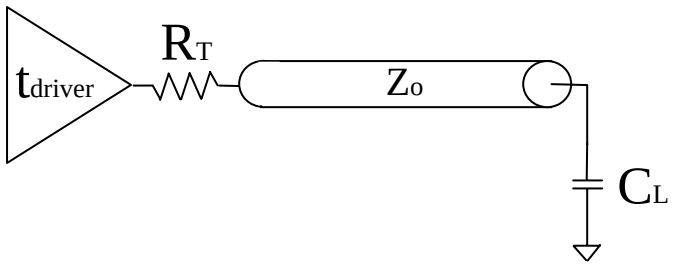
$t_{system} = \sqrt{(400p)^2 + (330p)^2}$ = 519 ps

$f_{max} = \dfrac{0.35}{519p}$ = **674 MHz**

PCB Bandwidth Estimation
(Series vs. Parallel Termination)

Series Termination Example

t_{driver} = 400 ps
$Z_o = R_L = 50\ \Omega$
C_L=6 pF



$Tau(\text{load}) = (50)*6p$ = 300 ps

$t_{rise}(\text{load}) = 2.2*(300p)$ = 660 ps

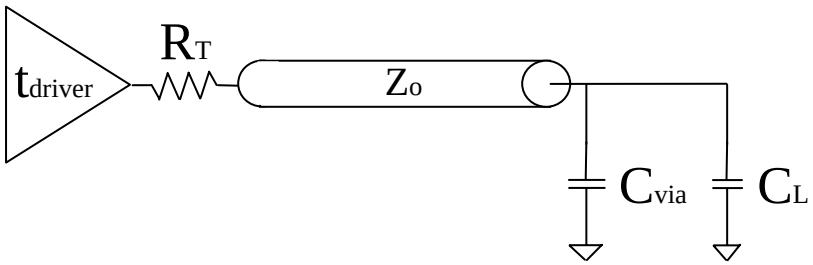
$t_{system} = \sqrt{(400p)^2 + (660p)^2}$ = 772 ps

$f_{\max} = \dfrac{0.35}{772p}$ = **454 MHz**

PCB Bandwidth Estimation
(Series vs. Parallel Termination)

Addition of a Via

t_{driver} = 400 ps
$Z_o = R_L = 50\ \Omega$
C_L=6 pF
C_{via} = 1pF



Tau(load) = (50)*6p	= 300 ps
t_{rise}(load) = 2.2*(300p)	= 660 ps
Tau(via) = (50)*1p	= 50 ps
t_{rise}(via) = 2.2*(50p)	= 110 ps
$t_{system} = \sqrt{(400p)^2 + (660p)^2 + (110p)^2}$	= 780 ps
$f_{max} = \frac{0.35}{780p}$	= **448 MHz**

- a loss of 7MHz due to the via

PCB Bandwidth Estimation
(Compensation)

1) **An inductor can be used in series w/ a capacitive load to raise the load impedance.**

2) **The ground plane clearance can be backed off around a via to make it look less capacitive.**

“RF Effects in PCB Design”

Comments or Question?