Novel 3-D Coaxial Interconnect System for Use in System-in-Package Applications

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***Abstract*—This paper presents the design and demonstration of a novel die-to-die interconnect system for deployment in system-in-package (SiP) applications with adjacent or stacked-die configurations. The interconnect system consists of miniature coaxial cables that are mounted to a standard Silicon substrate using an etched trench along the perimeter of the die. The trench serves as a self-alignment feature for both the signal and ground contacts in addition to providing mechanical strain relief for the coaxial cable. The system is designed to interface on-chip coplanar transmission lines to off-chip coaxial transmission lines to produce a fully impedance matched system. This approach promises to dramatically improve the electrical performance of high-speed, die-to-die signals by eliminating impedance discontinuities, providing a shielded signal path, and providing a low-impedance return path for the switching signal. The new interconnect system is designed to be selectively added to a standard wire bond pad configuration using an incremental etching process. This paper describes the design process for the new approach including the fabrication sequence to create the transition trenches. Finite-element analysis is performed to evaluate the electrical performance of the proposed system.**

***Index Terms*—Integrated circuit (IC) packaging, simultaneous switching noise (SSN), system-in-package (SiP), three-dimensional (3-D) chip stacking.**

I. Introduction

THE DEMAND for mobile computing products has driven the development of 3-D packaging techniques such as chip and package stacking [1]–[3]. Integrating multiple integrated circuit (IC) technologies into a system-in-package (SiP) has provided a way to achieve chip/package ratios greater than 200% [4]. The portable computing application requires functionally diverse technology such as complementary metal–oxide–semiconductor (CMOS), radio-frequency (RF), and passive components to be integrated into a single package, which is ideal for an SiP approach. The most widely used combination of technology in SiP is the integration of a CMOS processor and memory [5], [6]. The interconnection of the individual devices is typically accomplished using wire bonding. A wire bond provides a flexible approach to connecting arbitrary pad configurations and has been established as the most common package interconnect over the past decades [7]. While a wire bond provides a mechanically attractive solution to SiP interconnect, it has a host of electrical drawbacks [8], [9]. First, the high aspect ratio of the wire bond structure leads to a relatively high inductive property compared to the rest of the system. This becomes an issue as signaling speeds increase and the interconnect begins to behave as a distributed system [10]. When the interconnect behaves as a transmission line, then propagation delay and impedance discontinuities have to be considered. The wire bond tends to have very high characteristic impedance relative to the traditional 50 Ω system impedance. This impedance mismatch leads to reflections which may cause inadvertent switching of digital circuits. The second drawback of the wire bond is the unshielded nature of the structure. Electromagnetic (EM) field coupling between wire bonds leads to cross-talk noise on the signal lines. Finally, the inductive property of the wire bond causes simultaneous switching noise (SSN) when the return current from high-speed input/output (I/O) circuitry travels through the interconnect and induces ${}^{di}/_{dt}$ noise [11], [12].

The majority of work aimed at reducing the effect of impedance discontinuities and cross-talk in IC packaging has been focused on shrinking the interconnect structures to the point at which they do not behave as distributive elements [1]–[4]. While this approach has historically been sufficient, the nature of SiP creates a situation where long interconnect structures are unavoidable. Much work has also been done in the area of reducing SSN by using on-chip decoupling capacitors [11]. There is much interest in high dielectric materials for this application; however, this approach currently does not adequately reduce the majority of SSN from highly inductive interconnect. These factors drive the need for a new high speed interconnect structure for SiP.

The recent trend of using high speed serial busses for memory interfaces influences the development of a novel SiP interconnect system. The scaling of traditional off-chip, parallel busses becomes impractical due to electrical noise and cost. Instead, an approach of using a small number of high-speed lines to transmit serial data is being adopted. A new interconnect system should meet the following objectives: 1) provide controlled impedance to reduce reflections, 2) provide shielding for signal lines to reduce cross-talk, 3) provide a dedicated, low impedance return path to reduce SSN, and 4) be selectively added to a wire bonded system on a small number of high speed I/O lines.

In order to meet the above objectives, we propose a new coaxial interconnect system. The system uses miniature coaxial cables that interface to coplanar transmission lines on-chip. This approach provides matched impedance, EM shielding, and a dedicated return path. An anisotropic etching process is used to create trenches along the perimeter of the IC substrate in order

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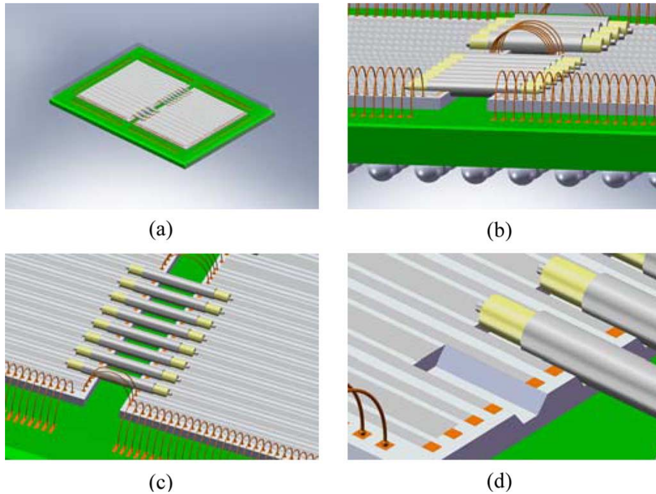

Fig. 1. Three-dimensional rendering of our interconnect approach used in an SiP application with adjacently placed dies. The coaxial cables are used in conjunction with wire bonds on high speed I/O lines. Images (a)–(c) show system from different perspectives while (d) shows the etched trench on the die with the cable removed.

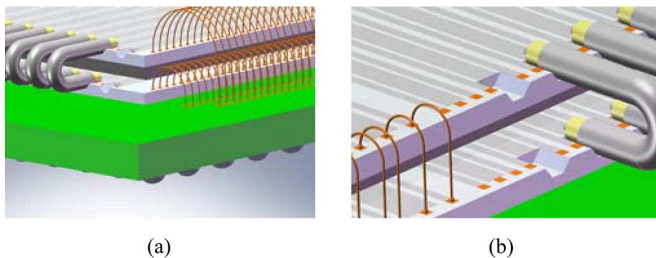

Fig. 2. Three-dimensional rendering of our interconnect approach used in an SiP application with stacked dies from different perspectives. Images (a) and (b) show the etched trenches on the die with the cable removed.

to align and strain relief the cables. This approach is designed to be selectively added to a perimeter bonded pad configuration on high speed I/O signals. This technique can be used on either adjacently placed or stacked-die SiP configurations.

II. Coaxial Interconnect System

Our interconnect system is accomplished by using semi-rigid, miniature coaxial cables that interface to on-chip coplanar transmission lines using an etched trench. The center conductor of the coaxial cable is exposed to make contact to the center trace of the coplanar signal trace while the outer shield of the semi-rigid cable makes contact with the two outer traces of the coplanar structure. Fig. 1 shows our proposed system used with adjacently placed dies. Fig. 2 shows our system used in a stacked die configuration.

A. Coaxial Cable Dimensions

The key dimensions that drive the design of the interconnect system are the features of the miniature coaxial cable. In our design, we have evaluated two versions of a miniature, semi-rigid, 50 Ω, coaxial cable from Micro-Coax [14]. The coaxial cable consists of a silver-plated, copper clad steel (SPCW) center conductor covered with an insulating layer of Polytetrafluoroethylene (PTFE). The outer conductor is created with a solid tubular layer of copper. The two semi-rigid coaxial cables that were evaluated in this work were the Micro-Coax UT-013 and the Micro-Coax UT-020 with overall diameters of 330 and 584 μm, respectively. Fig. 3 shows the variable names for the key dimensions of the coaxial cables used in our evaluation.

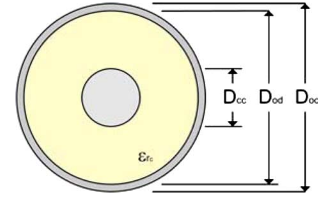

Fig. 3. Key dimensions for the coaxial cables.

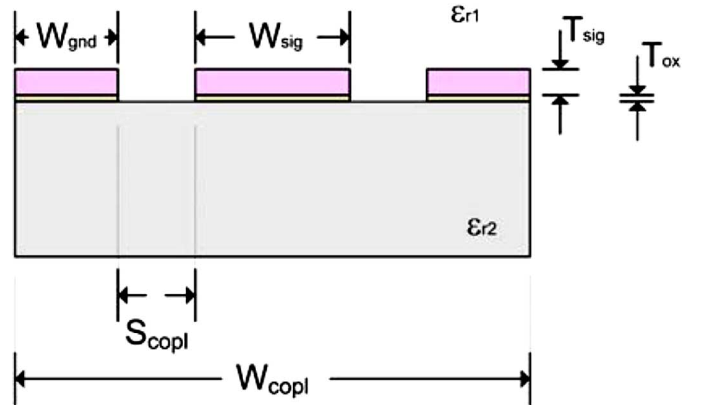

Fig. 4. Key dimensions for the on-chip coplanar transmission line.

B. Coplanar Dimensions

A coplanar transmission line is created using 3 traces of metal residing on the same plane. The inner trace carries the signal wave while the two outer traces carry the ground or return current. The width and thickness of the traces ($\mathrm{W_{sig}}, \mathrm{W_{gnd}}$, and $\mathrm{T_{sig}}$), the spacing between the traces ($\mathrm{S_{copl}}$), and the materials of the structure ($\varepsilon_{\mathrm{r1}}$ and $\varepsilon_{\mathrm{r2}}$) dictate the characteristic impedance of the transmission line. Fig. 4 shows a cross section of a coplanar transmission line fabricated on a p-type Silicon substrate. When constructing a coplanar structure on a p-type Silicon structure, a thin layer of Silicon Oxide (SiO_2) is inserted between the semiconductor substrate and the metal to provide a layer of adhesion and additional insulation ($\mathrm{T_{ox}}$). In our system, we used Aluminum to form the three traces used in the coplanar transmission line. The impedance of the structure was designed to be 50 Ω to match the impedance of the coaxial cable and eliminate reflections due to the off-chip interconnect path.

C. Trench Dimensions

A trench is formed within the coplanar structure such that the coaxial cable can be inserted and make electrical contact between the signal and ground conductors for both the coplanar and coaxial structures. The return path is accomplished by etching the trench within the coplanar structure but without removing any of the metal forming the two outer layer return traces. When the coaxial cable is laid in the trench, its outer

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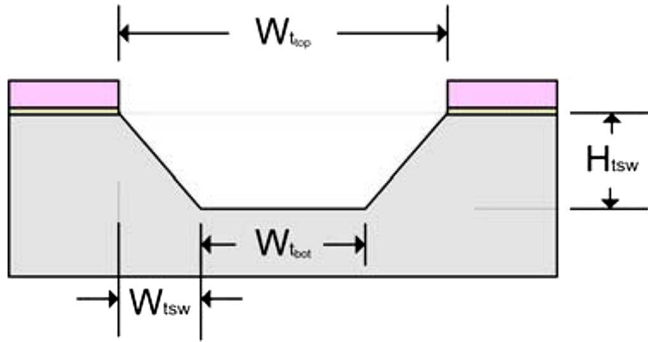

Fig. 5. Key dimensions for the etched trench.

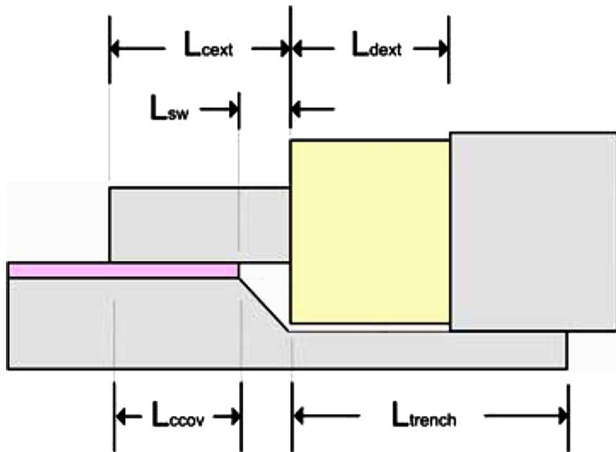

Fig. 6. Side view of the assembled interconnect system.

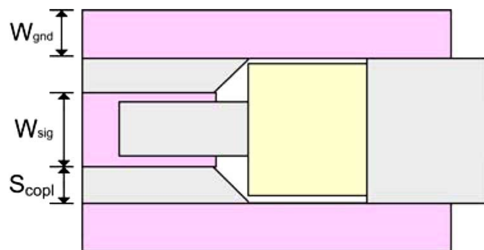

Fig. 7. Top view of the assembled interconnect system.

shield will be adjacent to the ground lines of the coplanar transmission line.

The signal path is formed by exposing the center conductor of the coaxial cable. When the coaxial cable is inserted into the trench, the center conductor will come to rest on top of the signal trace of the coplanar structure. The size of the coplanar transmission line (W_{sig}, W_{gnd}, and T_{sig}) and the size of the trench ($W_{ttop}, W_{tbot}, H_{tsw}$, and W_{tsw}) are designed to achieve both a 50 Ω impedance and the proper alignment of the coplanar to coaxial transition. Fig. 5 shows a cross section of the trench formed within the coplanar structure annotating the critical dimensions. Figs. 6 and 7 show side and top views of the assembled interconnect structure, respectively.

D. System Dimensions

Adjacent coplanar-to-coaxial structures can be placed on a pitch defined by S_{SS} as shown in Fig. 8. Table I lists all of the dimensions for our proposed technique for two sizes of miniature, semi-rigid coaxial cable (UT-013 and UT-020).

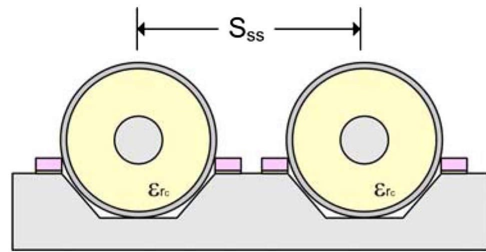

Fig. 8. Side view of two adjacent cables annotating the spacing.

TABLE I
DIMENSIONS FOR COPLANAR-TO-COAXIAL SYSTEM

Region	Parameter	Units	Coaxial Line	
			UT-013	UT-020
Coaxial (ε_{rc}=2.1)	D_{oc}	µm	330	584
	D_{od}	µm	254	419
	D_{cc}	µm	79	127
Coplanar (ε_{r1}=1) (ε_{r2}=11.7)	T_{sig}	µm	1	1
	T_{ox}	µm	1	1
	W_{sig}	µm	190	400
	W_{gnd}	µm	100	100
	S_{copl}	µm	65	85
	W_{copl}	µm	520	770
	S_{ss}	µm	620	870
Trench	W_{ttop}	µm	320	570
	W_{tbot}	µm	300	530
	W_{tsw}	µm	10	20
	H_{tsw}	µm	123.5	226.5
Transition	L_{trench}	µm	900	900
	L_{dext}	µm	400	400
	L_{sw}	µm	10	20
	L_{cext}	µm	100	100
	L_{ccov}	µm	90	80

This table illustrates the incremental area impact of our approach when compared to a typical wire bonded system. In a wire bonded system, a high speed net typically requires 3 bond pads in order to achieve a G-S-G configuration. The perimeter length required for this arrangement consists of the widths of the three wire bond pads (W_{pad}) plus the spacing between the pads (S_{pad}). Assuming a 100 μm × 100 μm bond pad ($W_{pad} = 100$ μm) with pad spacing of 100 μm ($S_{pad} = 100$ μm), the total distance required is $[3 \cdot \mathrm{Wpad} + 2 \cdot S_{pad}] = 500$ μm along the perimeter. In our approach, when using the UT-013 coaxial cable the total distance needed consists of the width of the top of the trench ($W_{ttop} = 349$ μm) plus the width of the two ground pads ($W_{pad} = 100$ μm). This gives a total perimeter length of $[W_{ttop} + 2 \cdot W_{pad}] = 549$ μm per signal. Our approach requires only a 9.8% increase in the perimeter length necessary to accommodate the coaxial-to-coplanar transition compared to the perimeter length needed for a traditional wire bonded G-S-G configuration.

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Another design consideration for this approach is the incremental weight associated with a coaxial interconnect. The Micro-Coax UT-13 coax cable has a weight of 400 μg/mm [14] compared to a traditional 25-μm-diameter gold wire bond with a weight of 10 μg/mm [25], or roughly 400 times more. Whether this increase in weight is tolerable will depend on the application but must be considered.

III. Fabrication of Trenches

A. Process Steps

We began with a 100-mm-diameter, p-type Silicon wafer with a $\langle 100 \rangle$ crystal orientation. The Si wafer is cleaned to remove any contamination using a modified RCA process. The cleaning process involves submerging the wafer in a sequence of three solutions. The first solution is a mixture of sulphuric acid and hydrogen peroxide to remove any organic material on the wafer. The second solution is a buffered oxide etch (BOE) consisting of a hydrofluoric acid diluted 10:1 with di-ionized (DI) water in order to remove any SiO_2. Finally a solution of hydrochloric acid, water, and hydrogen peroxide is used to remove any metal ions. In between each of these cleaning steps the wafer is rinsed in DI water. This step is reflected in Fig. 9(a).

The next set of process steps will etch the trench into the Si substrate. First, a protective layer of SiO_2 is grown on the wafer. The wafer is put into an oxidation furnace for 3 h at 1050 °C. This produces a layer of SiO_2 1 μm thick [Fig. 9(b)]. Next, a layer of *Shipley 1813* positive photo resist (PR) is spun onto the wafer. A 1-μm layer of PR is applied by spin coating the wafer at 5000 RPMs for 30 s. The PR is then hardened by baking the wafer for 90 s at 115 °C [Fig. 9(c)]. Photolithography is next performed using a dark field mask. The PR is exposed to UV light for 4.5 s at an intensity of 20 mW/cm^2 [Fig. 9(d)]. The PR is then developed by submersing the wafer in *MF 319 developer* solution for 60 s. The soluble PR is then removed using an acid wash. The remaining PR is hardened by a subsequent bake in order to make it resilient enough to withstand the forthcoming SiO_2 etch [Fig. 9(e)]. The SiO_2 is then etched using a BOE process [Fig. 9(f)]. The remaining PR is then stripped off using a sequence of acetone, isopropyl alcohol (IPA), methanol, and DI water [Fig. 9(g)]. The exposed Si substrate is etched using a Tetramethylammonium hydroxide (TMAH) solution at 25% weight [Fig. 9(h)]. This solution produces an anisotropic etch rate of 10.5 μm/hr at 75 °C for our $\langle 100 \rangle$ crystal orientation. TMAH also exhibited a 1/1000 selectability for SiO_2 at 75 °C so our 1 μm of SiO_2 is sufficient to protect the substrate for an etch depth up to 1000 μm. Finally, all remaining SiO_2 is stripped using a BOE process [Fig. 10(i)].

The next set of process steps deposit the metal used for the coplanar traces. First, the Si wafer is cleaned using the modified RCA process mentioned above. A 1-μm layer of SiO_2 is grown on the substrate using the same oxidation process mentioned above [Fig. 10(j)]. Next, Aluminum (Al) is deposited on the topside of the wafer using an evaporation process [Fig. 10(k)]. Photo resist is then applied [Fig. 10(l)] and a light field photolithography step is performed to expose selected regions of the PR [Fig. 10(m)]. The PR is developed and the soluble photo resist is removed [Fig. 10(n)]. The remaining PR is hardened with a subsequent bake. Next, the exposed Al is etched away using a sequence of Acetone, IPA, Methanol, and DI water [Fig. 10(o)]. Finally, all remaining SiO_2 is stripped using a BOE process [Fig. 10(p)].

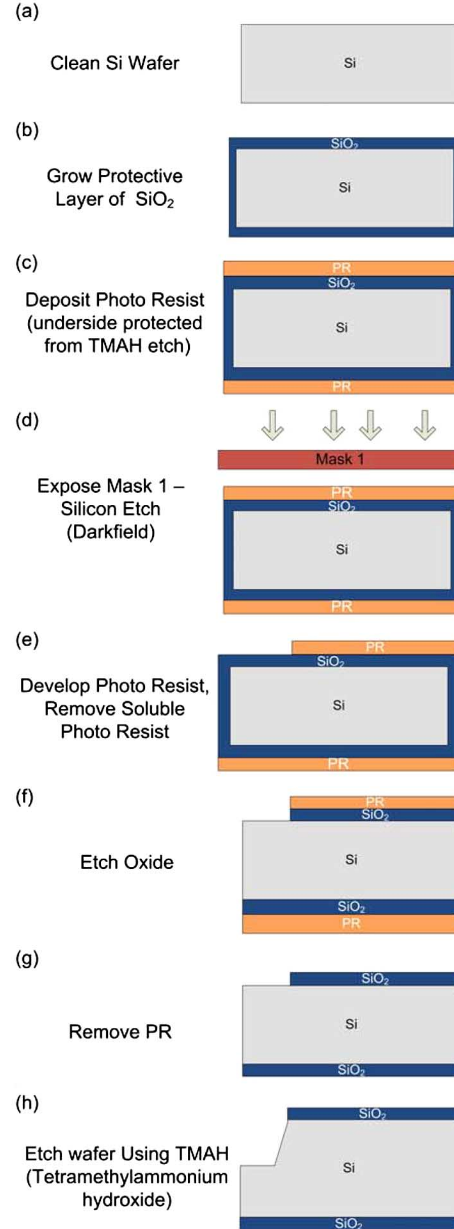

Fig. 9. Process steps (a)–(h) to create the transition trenches in Silicon.

B. Tolerance Analysis

An important consideration in moving to a new interconnect system is the analysis of the fabrication tolerances. In our system, the widest dimensional variance occurs in the trench fabrication. The coaxial cables used in our prototypes are specified to vary less than 0.0254 mm in the center and outer conductors diameters. This variance is considered insignificant relative to the size of the trench that the cable is laid into. The critical dimensions of the trench fabrication that effect assembly are the width $(\mathrm{W_{ttop}})$, the depth $(\mathrm{H_{tsw}})$, and the inward protrusion of the sidewall $(\mathrm{W_{tsw}})$. For our prototype fabrication process, we

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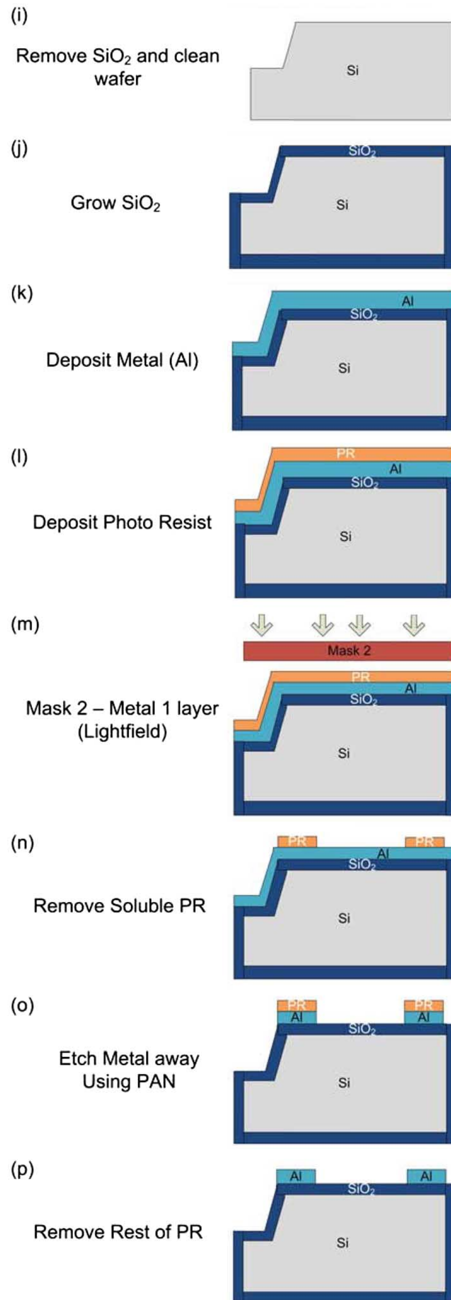

Fig. 10. Process steps (i)–(p) to create the coplanar transmission lines.

were able to hold the run-to-run variances of $\mathrm{W_{ttop}}$ and $\mathrm{H_{tsw}}$ to $+/-10\%$. The inward protrusion of $\mathrm{W_{tsw}}$ was held to less than a $+/-1\%$ variation due to the steep etching ratio (1/1000) achieved due to the Silicon crystal orientation.

The worst case scenario for a variance in $\mathrm{W_{ttop}}$ is that the trench is too narrow for the cable to be laid into. This situation is resolved by ensuring the minimum trench width is specified to always be greater than the outer diameter of the cable. The excess spacing between the outer conductors of the system is filled with conductive epoxy to ensure connectivity. Similarly, $\mathrm{H_{tsw}}$ is specified to always be shallow enough so that the cable center conductor is always vertically above the coplanar trace with any spacing being filled with epoxy.

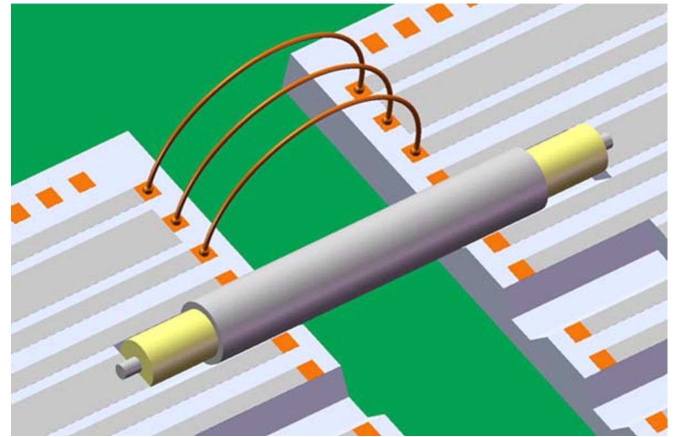

Fig. 11. Three-dimensional rendering of structures evaluated in the FEA analysis.

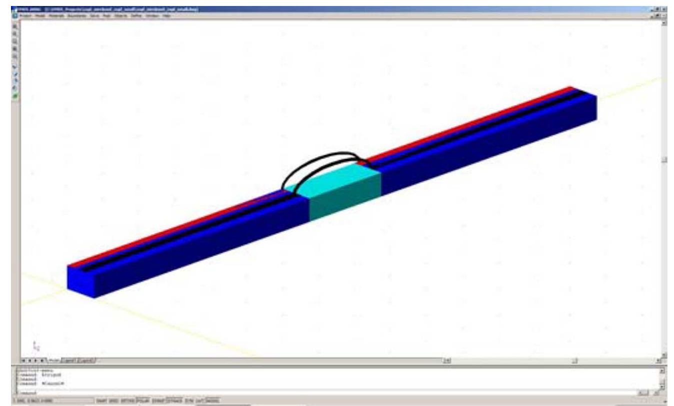

Fig. 12. Three-dimensional rendering of the wire bonded system in EMDS.

IV. Finite-Element Analysis (FEA) of Coplanar-to-Coaxial Electrical Performance

A. FEA Setup

In order to evaluate the electrical performance of the novel coaxial interconnect system, FEA was performed to extract the S-parameter data. The *Electromagnetic Design System (EMDS)* from *Agilent Technologies*, *Inc.* was used for the analysis. The coaxial system was compared to an equivalent system using wire bonds in order to evaluate the incremental electrical performance. Fig. 11 shows a 3-D rendering of the two interconnect system configurations that were evaluated. In the upper system, two adjacent dies containing 50-Ω coplanar transmission lines are connected using three, 25-μm-diameter, Aluminium wire bonds. The three wire bonds are necessary to connect the G-S-G configuration of the coplanar transmission lines. The lower configuration in Fig. 11 shows the coaxial interconnect system which connects the coplanar structures on the two adjacent dies. For both the wire bonded and coaxial interconnect systems, two miniature cable dimensions were used, the UT-013 and UT-020 (Table I). Figs. 12 and 13 show the FEA rendering of each system.

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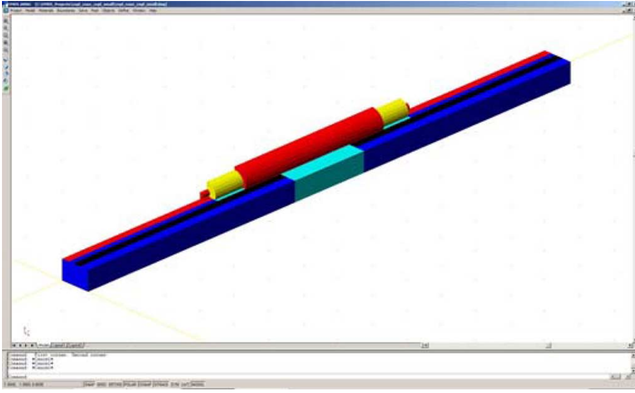

Fig. 13. Three-dimensional rendering of the coaxial system in EMDS.

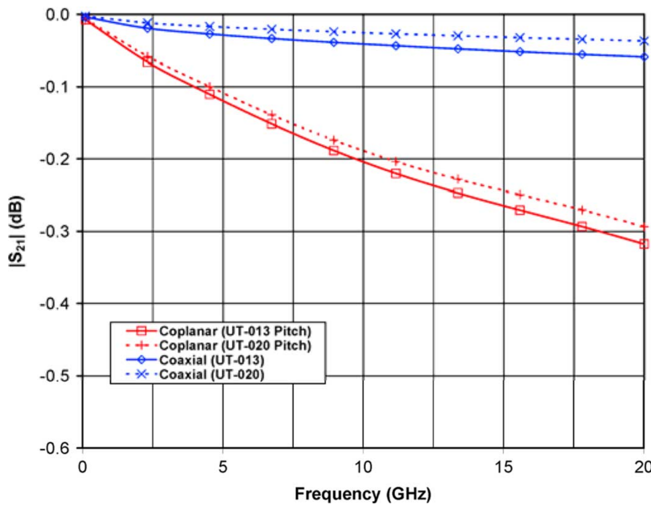

Fig. 14. $|S_{21}|$ response of 3 mm lengths of the two coplanar and two coaxial structures evaluated.

B. Transmission Line Loss

The first analysis that was performed was to evaluate the skin effect and dielectric loss of the transmission line structures used in the novel interconnect scheme. The frequency dependant loss in coaxial cables increases as the dimensions of the structure shrink. If the coaxial interconnect system is used to provide a high performance signal path compared to a wire bond, the loss in the cable itself needs to be insignificant. Also of importance is the loss in the on-chip coplanar transmission lines. The semiconductor substrate used for the coplanar lines causes the characteristic impedance to be complex. This is a concern not only for loss but for impedance matching to the coaxial cable. Two sizes of coplanar transmission lines were evaluated. The first structure was designed to accept the smaller UT-013 coaxial cable. The second was designed to accept the larger UT-020 coaxial cable. Figs. 14 and 15 show the magnitude of the S_{21} and S_{11} responses of 3 mm lengths of the two coplanar and two coaxial structures used in our system.

These plots show that for lengths of 3 mm, the transmission line structures proposed in this work have negligible loss ($|S_{21}| < -0.3$ dB @ 20 GHz) and provide a consistent impedance over the frequency range analyzed ($|S_{11}| < -23$ dB).

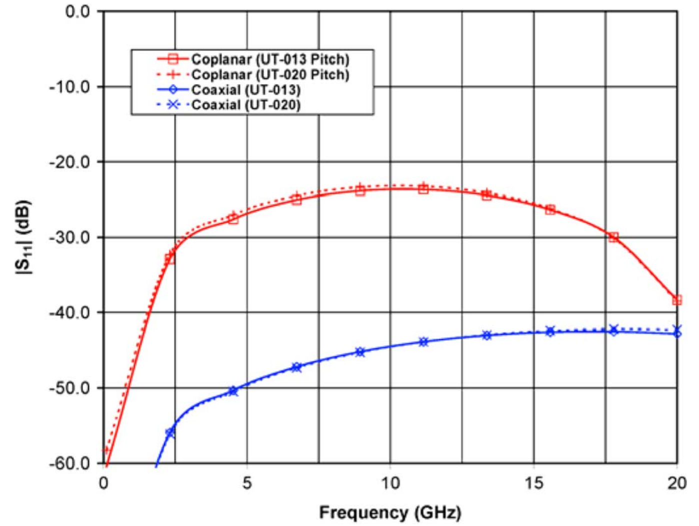

Fig. 15. $|S_{11}|$ response of 3 mm lengths of the two coplanar and two coaxial structures evaluated.

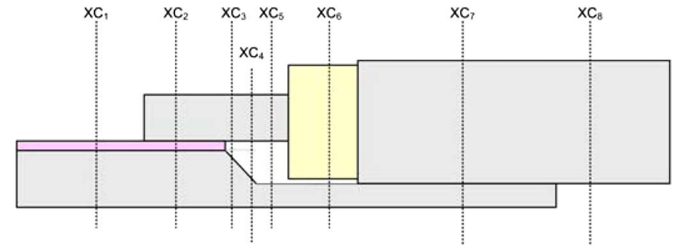

Fig. 16. Side view of the transition region from coplanar-to-coaxial with the locations of 8 distinct regions of different characteristic impedance.

C. Impedance Profile

The proposed system requires that an etched trench be used on the substrate to interface the coaxial structure to the coplanar transmission lines. In addition, the center conductor and dielectric of the coaxial cable must be exposed near the contact point in order to make the interconnect transition. This transition region is a source of impedance discontinuity as the signal traverses between the two controlled impedance structures. This transition region was analyzed in order to understand the impact of the manufacturing and assembly process of the proposed system on the impedance of the signal path.

There are eight distinct cross sections of the interconnect system. Each of these cross-sections has a different characteristic impedance dictated by the signal and return path and the dielectric materials that the EM fields traverse. Fig. 16 shows the side view of the transition region defining each of the cross sections. Fig. 17 shows the cross sections of the interconnect system at each of the definitions $(\mathrm{XC}_1 - \mathrm{XC}_8)$.

FEA was used to extract the characteristic impedance (Z_0) and the propagation constant (γ) for each of the eight cross sections in Fig. 17 at 10 GHz. The results are given in Table II.

D. System Performance

Finally, the entire interconnect system was evaluated using FEA. The analysis was performed for two wire bonded configurations corresponding to the pitch required to accept the two different sizes of coaxial cables evaluated (UT-013 pitch

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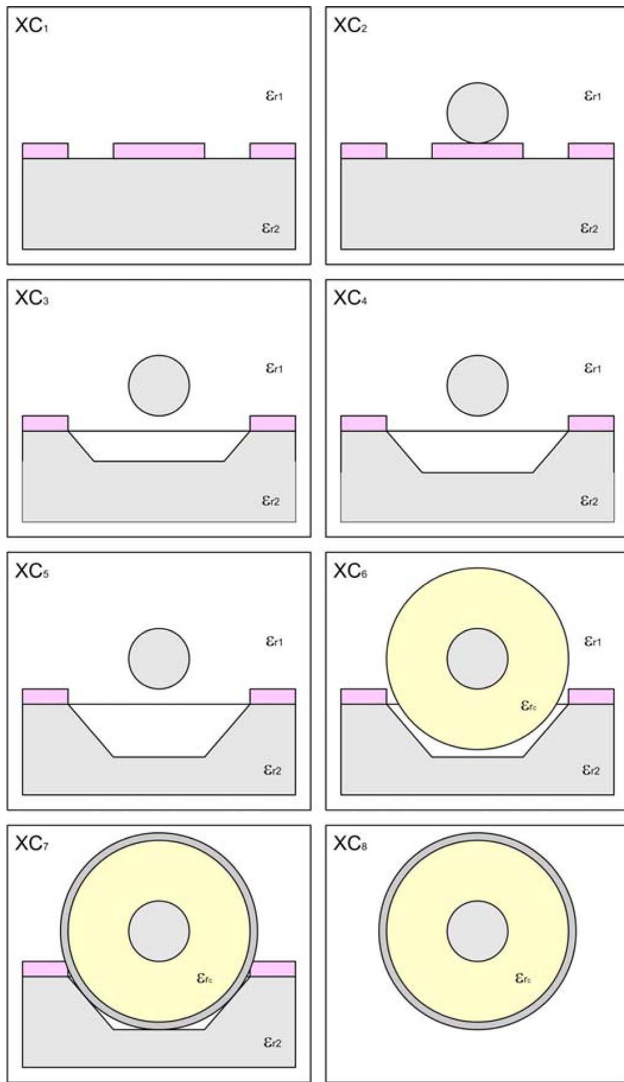

Fig. 17. Cross-sections of the eight distinct regions of different characteristic impedance in the coplanar-to-coaxial transition region.

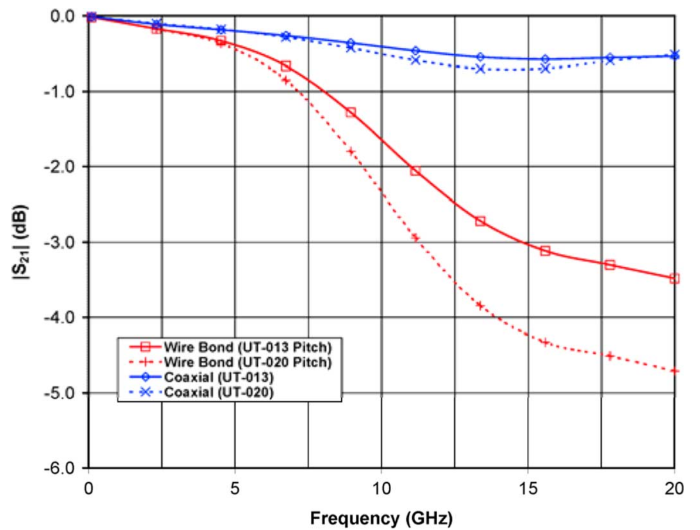

Fig. 18. $|S_{21}|$ response of the interconnect system comparing two wire bonded configurations to two coaxial configurations.

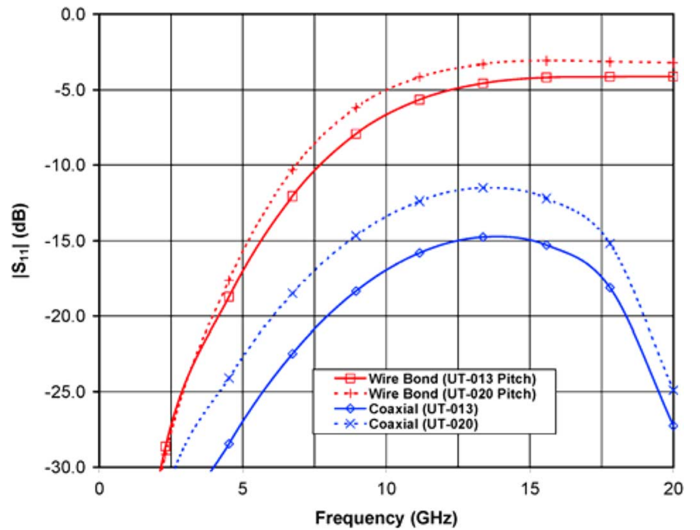

Fig. 19. $|S_{11}|$ response of the interconnect system comparing two wire bonded configurations to two coaxial configurations.

and UT-020 pitch). The analysis was then performed for the coplanar-to-coaxial system using the two different sizes of cables. Figs. 18 and 19 show the magnitude of the S_{21} and S_{11} responses of the four different interconnect configurations. The system consists of two, 3 mm coplanar lines on adjacent dies connected by a 3 mm coaxial cable in order to traverse the 1 mm spacing between dies (shown in Fig. 11).

These plots demonstrate the dramatic increase in electrical performance that the coaxial interconnect system achieves compared to the traditional wire bond approach. The transmitted response ($|S_{21}|$) of the coaxial system exhibits less than -0.7 dB of loss across the entire frequency range from dc to 20 GHz. This is compared to the wire bond which falls beneath the -3 dB point between 10 and 15 GHz.

E. Transient Analysis

The S-parameters were used to create a transient simulation in order to observe the eye diagram of a representative digital signal. The wire bonded (UT-013 pitch) system was compared to the UT-013 coaxial system. The interconnect systems were stimulated with a $2^8 - 1$ Pseudo Random Bit Sequence (PRBS) running at 5 Gb/s with a 35 ps rise time. Fig. 20 shows the transmitted eye diagram of the wire bonded system. Fig. 21 shows the eye diagram of the coaxial system. The impedance discontinuities and parasitics of the wire bonds result in reflections and rise time degradation which is apparent in the eye diagram shown in Fig. 20. The signal degradation is almost completely eliminated in the coaxial system due to the controlled impedance nature of the structures. The small reflections observed in Fig. 21 are due to the transition regions but result in less than 5% of electrical noise.

V. Experimental Results

A. Prototype Fabrication

A test chip was fabricated at the Montana Microfabrication Laboratory (MML) at Montana State University, Bozeman, in order to evaluate the feasibility of creating the transition

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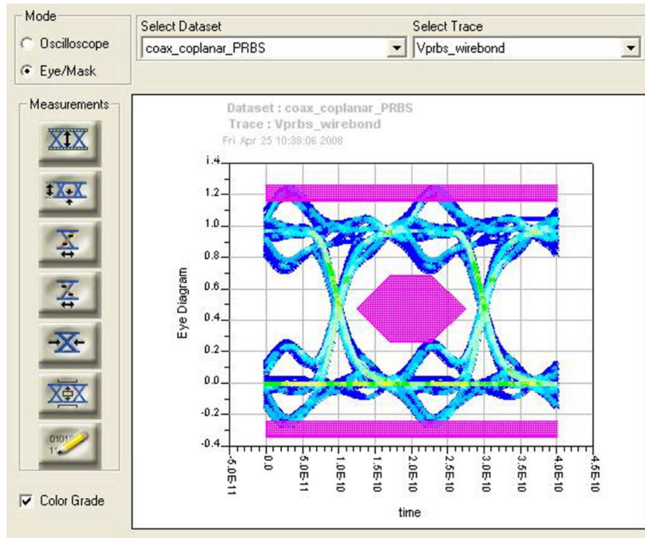

Fig. 20. Transmitted eye diagram of the wire bonded (UT-013 pitch) system.

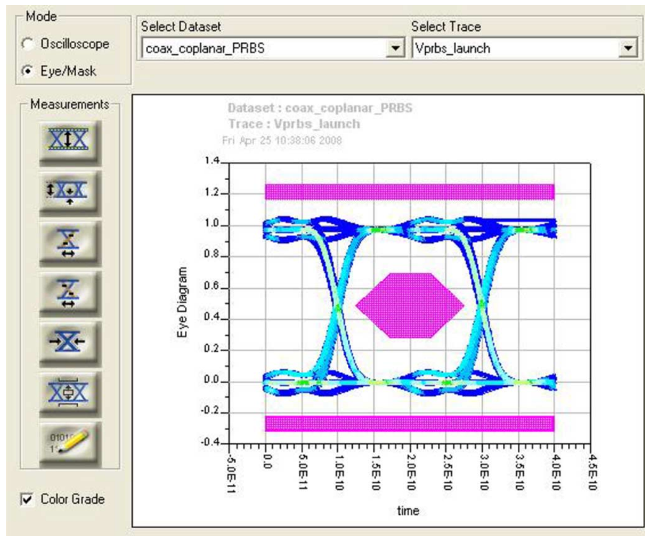

Fig. 21. Transmitted eye diagram of the coaxial (UT-013) system.

trenches for the coaxial system in Silicon. The process steps described in Section III were used to produce a physical prototype. Fig. 22 shows the top view of the prototype die. Fig. 22(a) and (b) show the coplanar transmission line structures. Fig. 22(c) and (d) show the etched trenches. The coplanar structures shown in this figure are for the UT-13 cable trench with dimensions given in Table I. The coplanar structures were fabricated with a 100 μm separation between outer ground traces, thus yielding a cable-to-cable pitch of 620 μm.

A test fixture was created in order to evaluate various assembly methods in addition to future electrical evaluation. The test fixture is shown in Fig. 23 and is loaded with nine of the prototype dies. This fixture allows the evaluation of adjacently placed and stacked-die configurations using either a wire bonded or coaxial interconnect approach. Figs. 24 and 25 show a prototype assembly showing the miniature coaxial cables attached to adjacently placed dies.

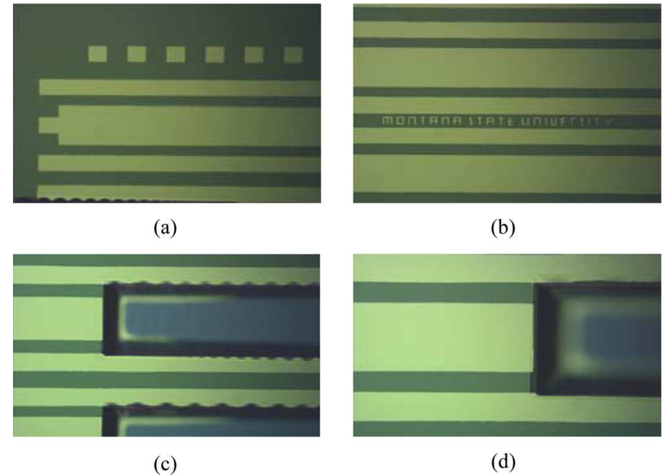

Fig. 22. Top view of our prototype die showing the coplanar transmission lines (a) and (b) and the etched trenches for the coaxial cables (c) and (d).

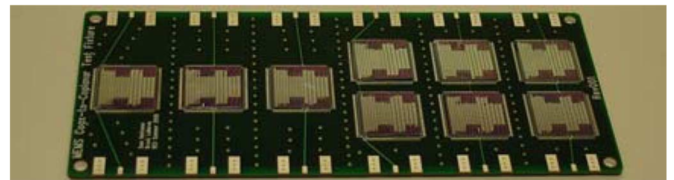

Fig. 23. Test fixture for assembly development and electrical evaluation.

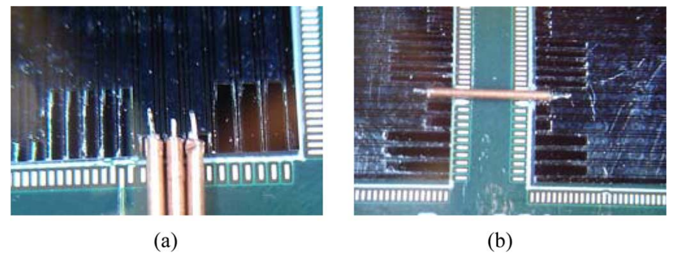

Fig. 24. Prototype assembly of adjacently placed dies.

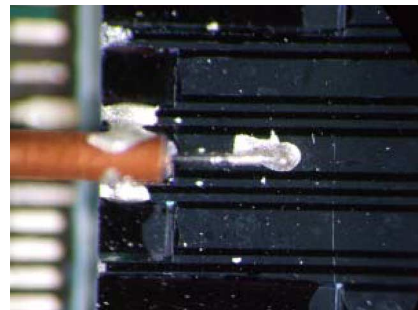

Fig. 25. Measurement setup used to test the interconnect system.

B. Assembly

The assembly for this system has been initially accomplished using a conductive epoxy. The semi rigid coaxial cable is stripped to expose its center conductor and inner dielectric. The coaxial cable is laid into the etched trench on the Silicon such that the cable center conductor rests on top of the coplanar center trace. A small amount of conductive epoxy is applied to form the bond between the conductors. When the cable is

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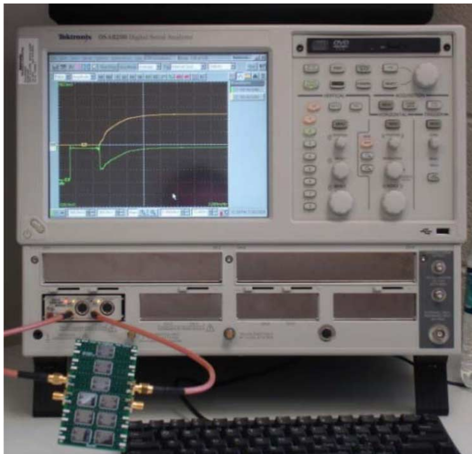

Fig. 26. Measurement setup used to test the interconnect system.

laid into the trench, its outer shield is positioned between the two outer traces of the trench. A small amount of conductive epoxy is brushed across the ground conductors to form the return path. This type of assembly process provides a low resistance bonding mechanism which can be automated on a select number of signals. An automated epoxy application system can be developed which is similar to the underfill process used in flip-chip assembly.

The adhesive investigated for the initial prototype was an *EPO-TEK H2OE* [20] which is a two component, silver based epoxy designed for microelectric applications. The volume resistivity of *EPO-TEK* is less than 0.4 m Ohm-cm at 23 °C. The epoxy has a cure time of 15 min at 120 °C or 5 min at 150 °C. This particular epoxy was chosen due to its commercial availability. A high volume application would require an epoxy with a lower cure time. Further investigation into mechanical reliability under thermal stresses is also necessary for adoption into a manufacturing environment. The following figure shows a top view of the prototype coaxial-to-coplanar assembly using conductive epoxy.

C. Electrical Measurement Results

The interconnect system was tested with *Time Domain Reflectrometry (TDR) and Time Domain Transmission (TDT)* using the *Tektronix DSA8200* sampling oscilloscope with an 80E04 TDR modules. This test setup is capable of stimulating the interconnect system with a step of 35 ps and observe the reflected energy (TDR) and the transmitted energy (TDT). Fig. 26 shows the experimental setup used to test the interconnect system.

TDR and TDT measurements were taken on a wire bonded system first so a comparison of electrical performance could be made. Figs. 27 and 28 show the TDR and TDT measurements respectively of two adjacently placed dies connected together using wire bonds to make the G-S-G connection on the wide coplanar transmission line and the UT-20 coaxial cable. An equivalent simulation model was created to model the electrical behavior of the elements within the measurement. The response of the model is overlaid on the measurement data to verify its correlation.

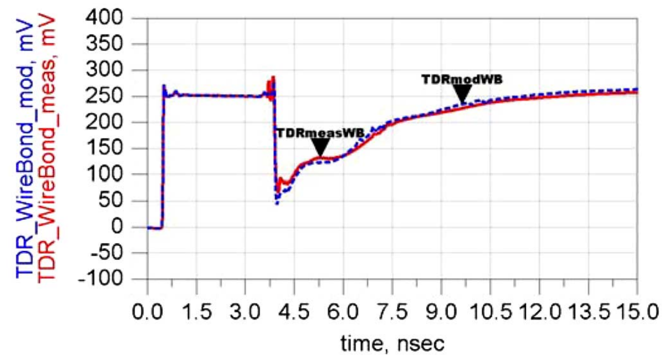

Fig. 27. TDR Measurement of a wire bonded system.

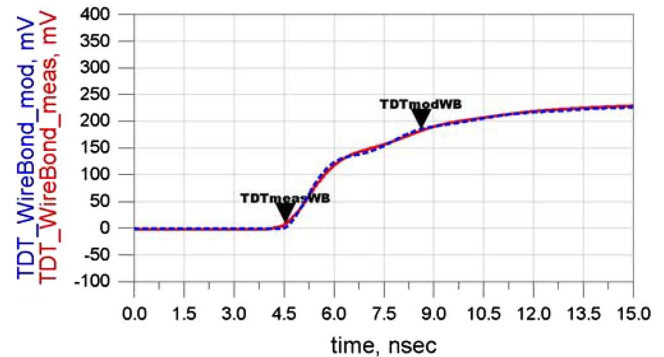

Fig. 28. TDT Measurement of a wire bonded system.

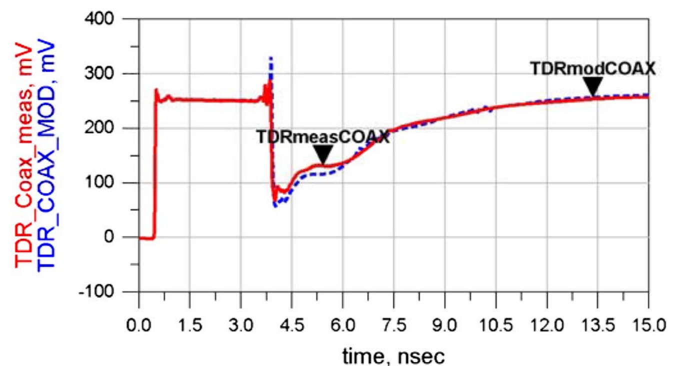

Fig. 29. TDR Measurement of the coaxial system.

The wire bonds were then removed from the dies and the coaxial cable was then connected using the assembly process described above. Figs. 29 and 30 show the TDR and TDT measurements respectively of two adjacently placed dies connected together using the UT-20 coaxial cable. Again, an equivalent circuit model was created to mimic the behavior of the system. The models response is overlaid on the measurement data to verify its correlation.

The measurements of the interconnect system showed that the response was dominated by the loss in the long coplanar transmission lines. In order to isolate the response of just the interconnect, the equivalent circuit models were used. The model of the lossy coplanar lines was removed from the simulation model in addition to the effects of the DUT and instrument cables. The remaining circuit model was for only the interconnect system

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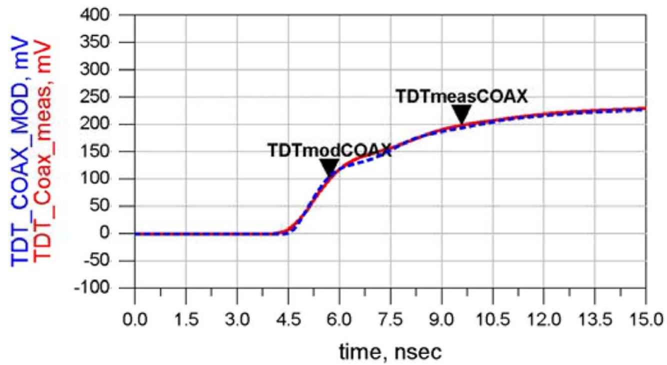

Fig. 30. TDT Measurement of the coaxial system.

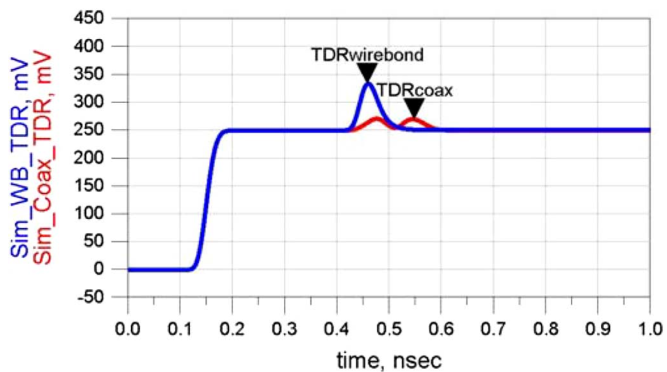

Fig. 31. Simulated TDR comparing the wire bond and coaxial interconnect responses.

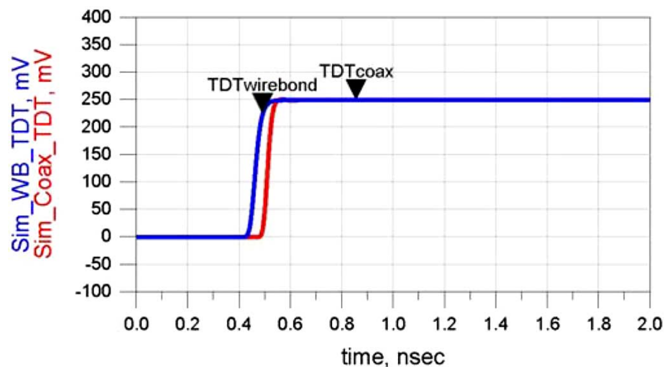

Fig. 32. Simulated TDT comparing the wire bond and coaxial interconnect responses.

and allowed a true comparison of the electrical performance of the wire bond to the coaxial system. Figs. 31 and 32 show a simulated TDR and TDT respectively of the simulated responses of just the interconnect systems.

The responses of just the interconnect (Figs. 31 and 32) demonstrate a significant improvement in electrical performance by moving toward a coaxial system. The wire bond resulted in a 33% reflection when stimulated with a 35 ps step. When using a coaxial interconnect instead, the reflection was reduced to 8%. The 10–90 rise time of the wire bonded system was found to be 49 ps. The 10–90 rise time of the coaxial

TABLE II
Z_0 AND γ FOR THE CROSS SECTIONS DEFINED IN FIG. 16

Region	Z_0 (Ω)	g (Np/m + j (rad/m))
XC_1	52 + j26	305 + j615
XC_2	50 + j25	299 + j604
XC_3	114 + j3	10 + j269
XC_4	128 + j1	4 + j239
XC_5	134 + j1	3 + j229
XC_6	111 + j1	5 + j276
XC_7	50 + j0	0 + j296
XC_8	50 + j0	0 + j296

system was found to be 38 ps. These improvements are due to the reduction of the parasitic inductance of the interconnect by moving toward a coaxial structure.

VI. Future Work

Work is currently underway to develop an automated assembly process and to evaluate the reliability of the coaxial interconnect connections.

VII. Conclusion

In this paper we presented a novel coaxial interconnect system for use in 3-D SiP packaging. The interconnect system is designed to be selectively added to a traditional wire bond pad configuration on a small number of critical, high speed nets using an incremental etching step. This approach delivers a significant increase in electrical performance compared to a wire bond used in the same configuration. This novel system promises to meet the performance needs of future high density IC packaging applications.

Acknowledgment

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References

[1] B.-W. Lee, J.-Y. Tsai, H. Jin, C. K. Yoon, and R. R. Tummala, "New 3-E chip stacking architectures by wire-on-bump and bump-on-flex," *IEEE Trans. Adv. Packag.*, vol. 31, no. 2, pp. 367–376, May 2008.

[2] V. Kripesh, S. W. Yoon, V. P. Ganesh, N. Khan, M. D. Rotaru, F. Wang, and M. K. Iyer, "Three-dimensional system-in-package using stacked silicon platform technology," *IEEE Trans. Adv. Packag.*, vol. 28, no. 3, pp. 377–386, Aug. 2005.

[3] R. M. Lea, I. P. Jalowiecki, D. K. Boughton, J. S. Yamaguchi, A. A. Pepe, V. H. Ozguz, and J. C. Carson, "A 3-D stacked chip packaging solution for miniaturized massively parallel processing," *IEEE Trans. Adv. Packag.*, vol. 22, no. 3, pp. 424–432, Aug. 1999.

[4] M. Karnezos, "3D packaging: Where all technologies come together," in *Proc. IEEE/CPMT/SEMI 29th Int. Electron. Manufact. Technol. Symp.*, Jul. 2004, pp. 64–67.

Authorized licensed use limited to: MONTANA STATE UNIV BOZEMAN. Downloaded on March 10,2010 at 18:23:29 EST from IEEE Xplore. Restrictions apply.

[5] K. Nakazato, "Future memory devices—From stacked memory, gain memory, single-electron memory to molecular memory," in *Proc. 2006 Int. Symp. VLSI Technol., Syst., Appl.*, Apr. 2006, pp. 1–2.

[6] D. J. Wouters, "Moving away from silicon: The role of interconnect in new memory technologies," in *Proc. IEEE Int. Interconnect Technol. Conf.*, Burlingame, CA, Jun. 4–6, 2007, pp. 169–171.

[7] Y. T. Lin, C. T. Peng, and K. N. Chiang, "Parametric design and reliability analysis of wire interconnect technology wafer level packaging," *J. Electron. Packag.*, vol. 124, no. 3, pp. 234–239, Sep. 2002.

[8] E. McGibney and J. Barrett, "An overview of electrical characterization techniques and theory for IC packages and interconnects," *IEEE Trans. Adv. Packag.*, vol. 29, no. 1, pp. 131–139, Feb. 2006.

[9] D. Kam and J. Kim, "40-Gb/s package design using wire-bonded plastic ball grid array," *IEEE Trans. Adv. Packag.*, vol. 31, no. 2, pp. 258–266, May 2008.

[10] R. H. Caverly, "Characteristic impedance of integrated circuit bond wires (short paper)," *IEEE Trans. Microwave Theory Tech.*, vol. 34, no. 9, pp. 982–984, Sep. 1986.

[11] C. Ryu, J. Park, J. S. Pak, K. Lee, T. Oh, and J. Kim, "Suppression of power/ground inductive impedance and simultaneous switching noise using silicon through-via in a 3-D stacked chip package," *IEEE Microwave Wireless Compon. Lett.*, vol. 17, no. 12, pp. 855–857, Dec. 2007.

[12] H.-F. Huang, Q.-X. Chu, and J.-K. Xiao, "Microstrip mismatching technique for reducing SSN in high speed integrated circuit," *IEEE Trans. Compon. Packag. Technol.*, vol. 31, no. 2, pp. 439–443, Jun. 2008.

[13] B. Mutnury, M. Cases, P. Nam, D. N. de Araujo, E. Matoglu, P. Patel, and B. Herrman, "Analysis of fully buffered DIMM interface in high-speed server applications," in *Proc. 56th Electron. Compon. Technol. Conf.*, May 2006, pp. 203–208.

[14] UT-013/UT-020 Data Sheet [Online]. Available: http://www.micro-coax.com

[15] B. LaMeres and C. McIntosh, "Off-chip coaxial to microstrip transition using MEMS trench," presented at the NASA Symp. VLSI Design, Post Falls, ID, Jun. 2007.

[16] C. McIntosh and B. LaMeres, "Fab process for high speed coaxial to coplanar off-chip interconnect," presented at the Electron. Syst.-Integration Technol. Conf., London, U.K., Sep. 1–4, 2008.

[17] W. Dally and J. Poulton, *Digital Systems Engineering*. New York: Cambridge Univ. Press, 1998.

[18] E. Bogatin, *Signal Integrity—Simplified*. Upper Saddle River, NJ: Prentice-Hall, 2003.

[19] The International Technology Roadmap for Semiconductors Tech. Rep., 2007 [Online]. Available: http://www.itrs.net

[20] Conductive silver-epoxy data sheet [Online]. Available: http://www.tedpella.com

[21] S. Tomiyama and Y. Fukui, "Gold bonding wire for semiconductor applications," *J. Gold Sci., Technol., Appl.*, vol. 15, no. 2, Mar. 1982.

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