National Aeronautics and Space Administration

Error Mitigation of Point-to-Point Communication for Fault-Tolerant Computing

Authors: Robert L Akamine, Robert F. Hodson, Brock J. LaMeres, and Robert E. Ray

Contents

- Introduction to the Problem
- Solution Strategies
- Advantages and Disadvantages to each Strategy
- Suggested Applications

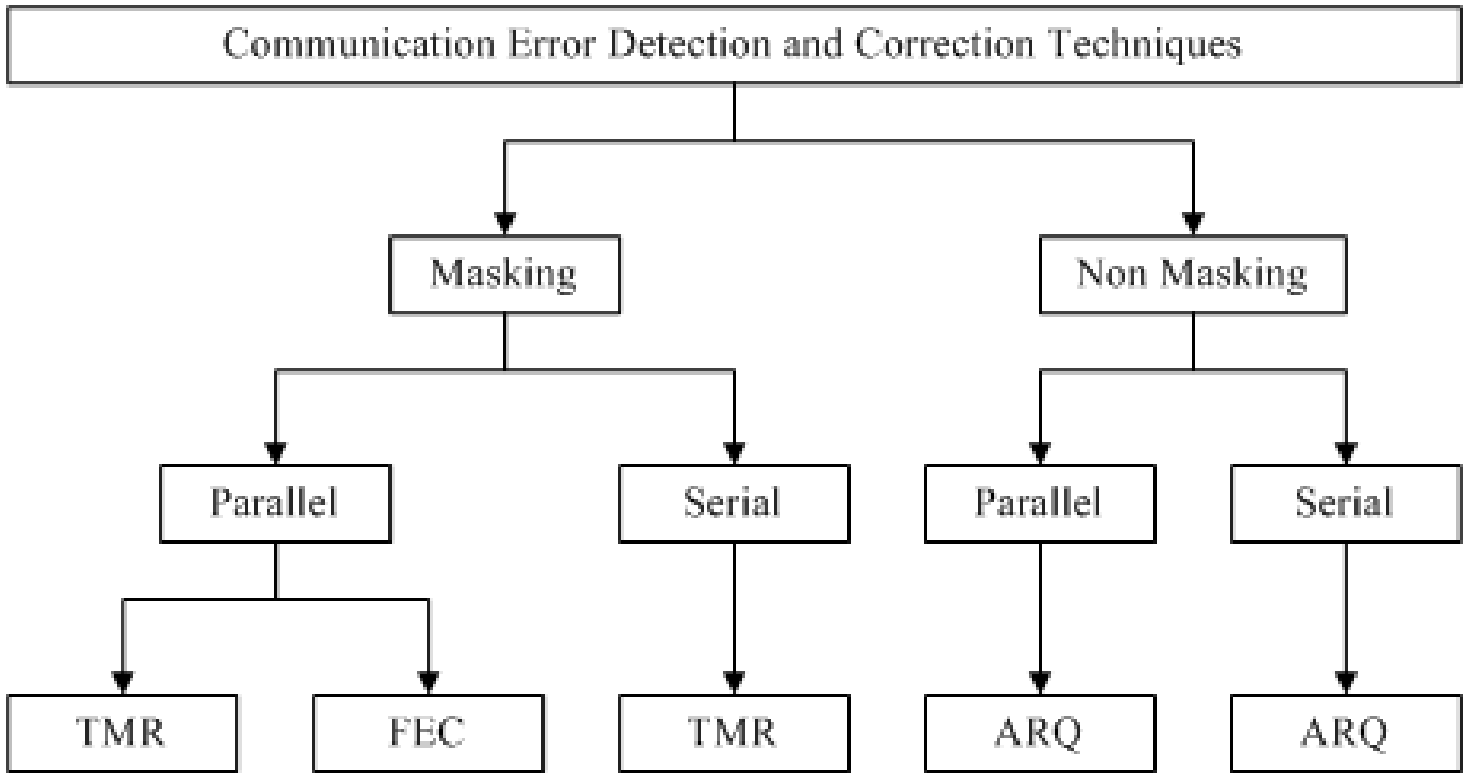
Introduction to the Problem

- How to detect and recover from physical damage or ‘glitches’ between two communication points
- Physical damage can be caused by ;
  - Impact from debris
  - Damage from use
- ‘Glitches’ refer to Single Event Upsets (SEU) and Single Event Transients (SET)
- Important problem for space and military applications
- Even more important since Commercial Off The Shelf (COTS) parts are being used in more rugged environments
  - COTS parts have higher performance and cost less than radiation hardened parts

Solution Strategies

- Two main types of methods detect and recover from disrupted or disabled communication lines
  - Masking – Detecting, isolating, and recovering from errors in real-time
  - Non-masking – Errors are detected in real-time. However, communication needs to halt to isolate and recover from errors
- Masking example
  - Forward Error Correction (FEC) codes and Triple Modular Redundancy (TMR)
- Non-masking example
  - Automatic Repeat Query (ARQ) – A command and response protocol. The transmitter sends data and expects an acknowledgement from the receiver
  - Uses parity, Cyclic Redundancy Checks (CRC), or other Error Detection Codes (EDC) to detect errors

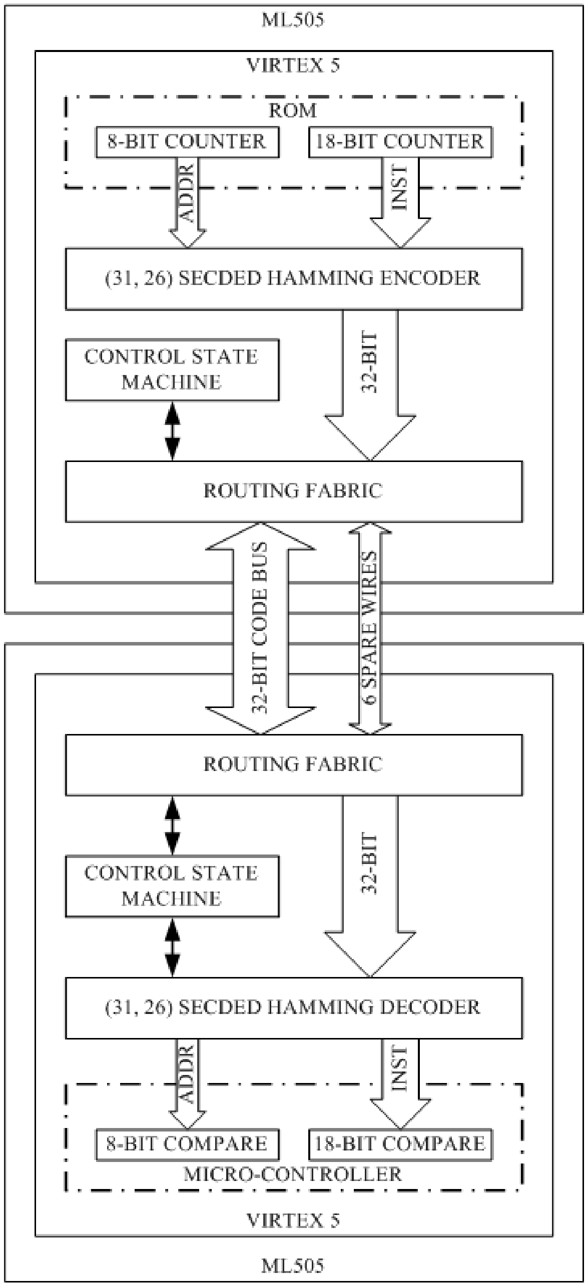
Solution Strategies



Solution Strategies - FEC

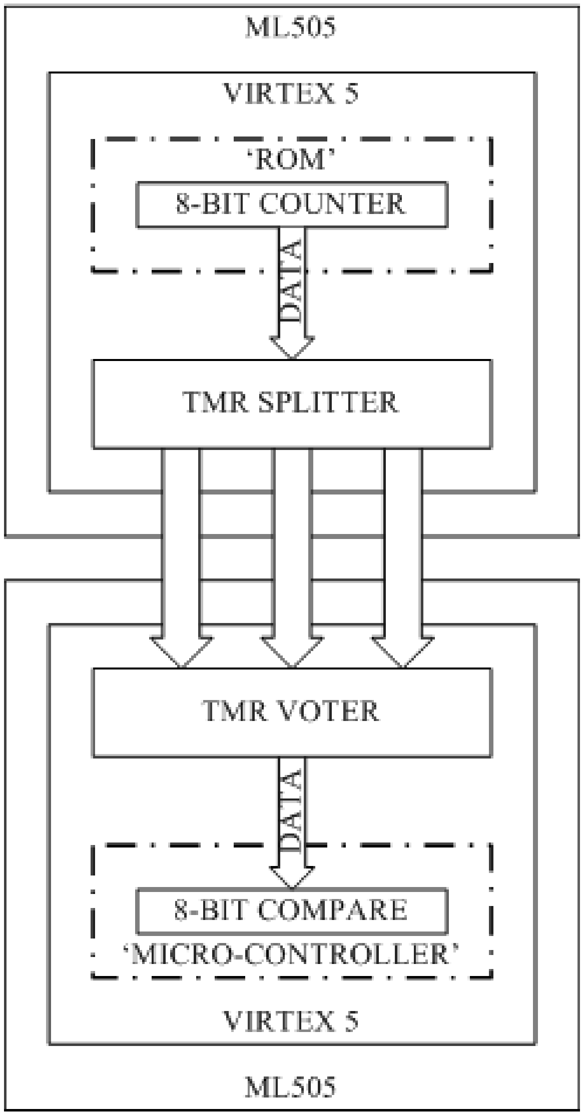
- Montana State Hamming code demonstration
- Uses Hamming codes to detect and correct a single bit error and detect two errors

  Limits Hamming to working with only one error condition (physical damage or SEU)
- Included a ARQ type protocol to switch from damaged to undamaged wires
- Meant to emulate communication between ROM and a microcontroller
- Demonstration implemented on Xilinx ML-505 Virtex-5 FPGA development boards



Solution Strategies - TMR

- TMR is a simple masking technique where the transmitter replicates the same data three times and the receiver votes to decide what is valid data
- The probability of two SEU’s causing erroneous data to exit the voter is very low
- The probability of two damaged wires affecting the same three bit cluster is low
- Demonstration implemented on Xilinx ML-505 Virtex-5 FPGA development boards

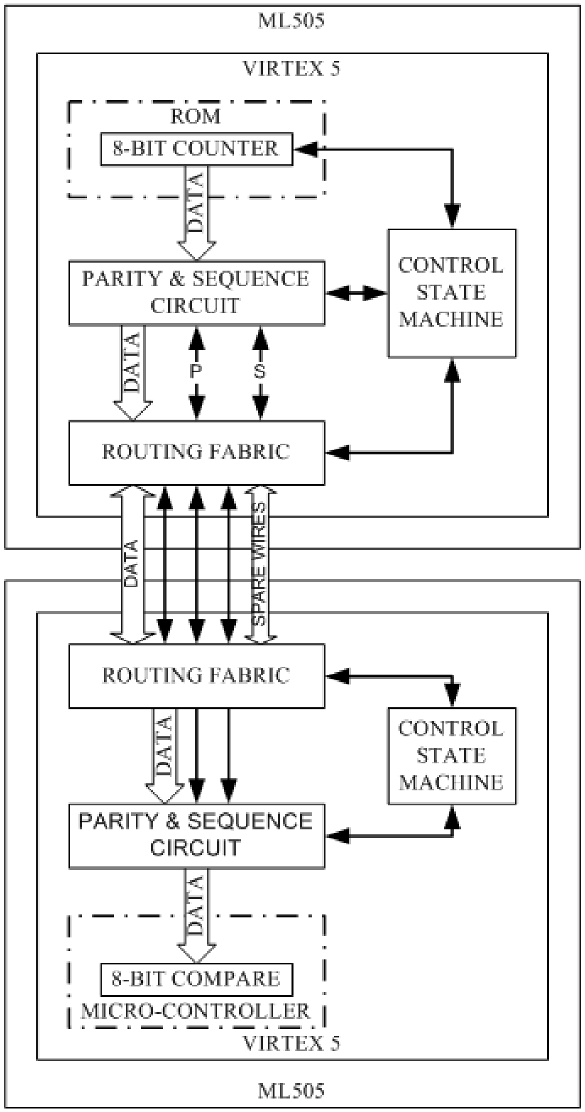


Solution Strategies – ARQ with Parity

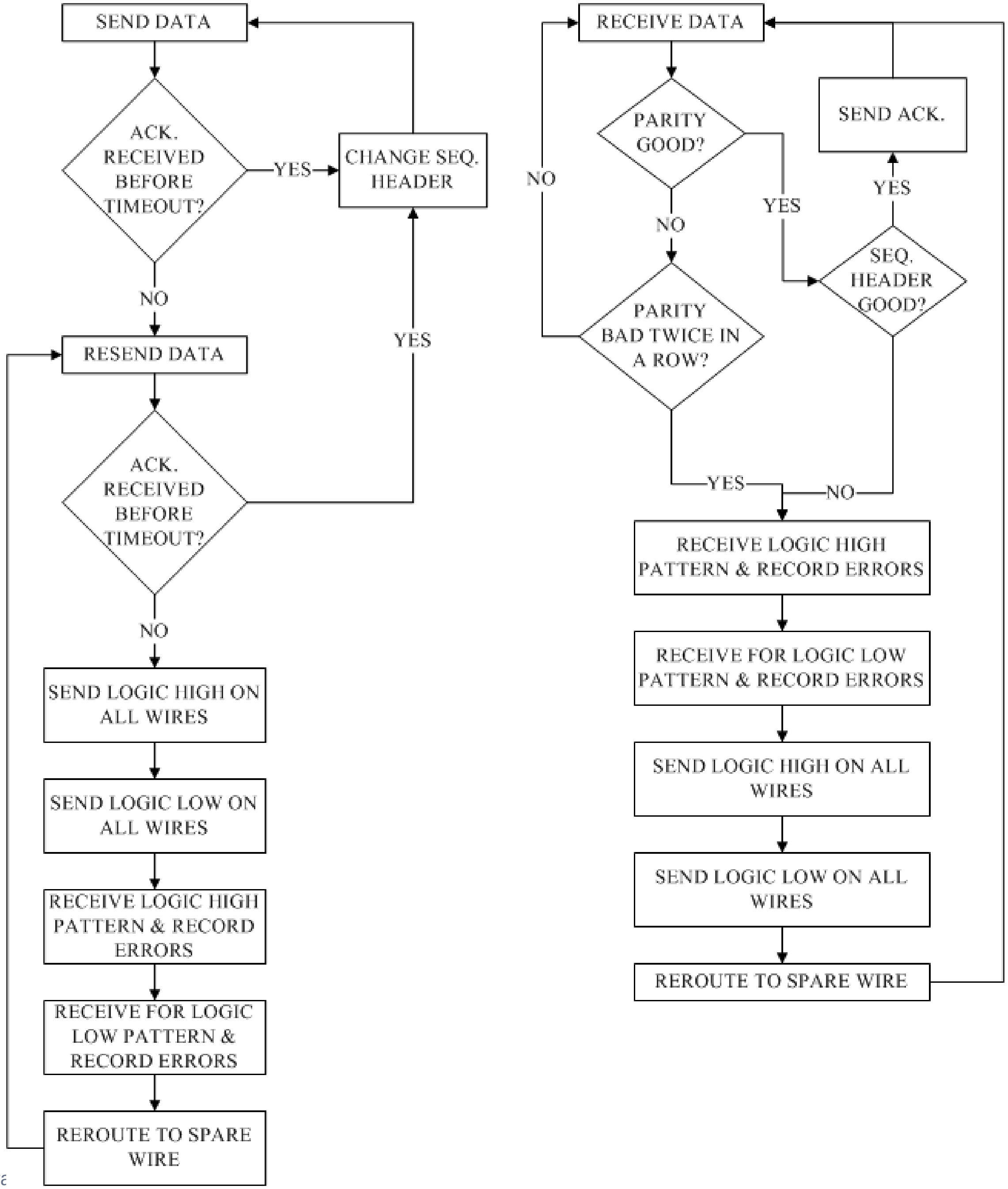
- Errors are detected with simple parity
- Data is sent with a parity bit and an additional sequence bit from the transmitter to the receiver

  The sequence bit allows the receiver to know if data was repeated.

- The transmitter expects an acknowledgement from the receiver in order to continue communication
- In the case of a single case of bad parity cause by an SEU data is retransmitted
- If damaged wired are detected the affected data, parity, or sequence bit is rerouted to spare wires



Solution Strategies – ARQ with Parity

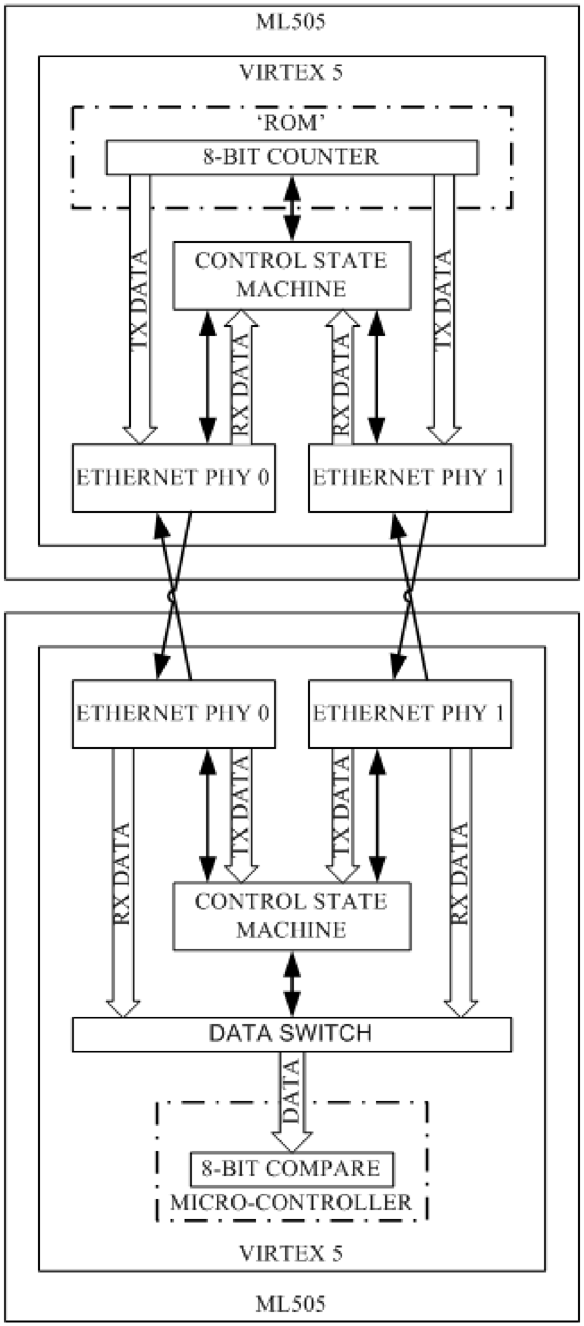

SEND DATA
ACK. RECEIVED BEFORE TIMEOUT?
YES
CHANGE SEQ. HEADER
NO
RESEND DATA
YES
ACK. RECEIVED BEFORE TIMEOUT?
NO
SEND LOGIC HIGH ON ALL WIRES
SEND LOGIC LOW ON ALL WIRES
RECEIVE LOGIC HIGH PATTERN & RECORD ERRORS
RECEIVE FOR LOGIC LOW PATTERN & RECORD ERRORS
REROUTE TO SPARE WIRE
RECEIVE DATA
PARITY GOOD?
SEND ACK.
NO
YES
YES
NO
SEQ. HEADER GOOD?
PARITY BAD TWICE IN A ROW?
YES
NO
RECEIVE LOGIC HIGH PATTERN & RECORD ERRORS
RECEIVE FOR LOGIC LOW PATTERN & RECORD ERRORS
SEND LOGIC HIGH ON ALL WIRES
SEND LOGIC LOW ON ALL WIRES
REROUTE TO SPARE WIRE

Solution Strategies – Ethernet ARQ

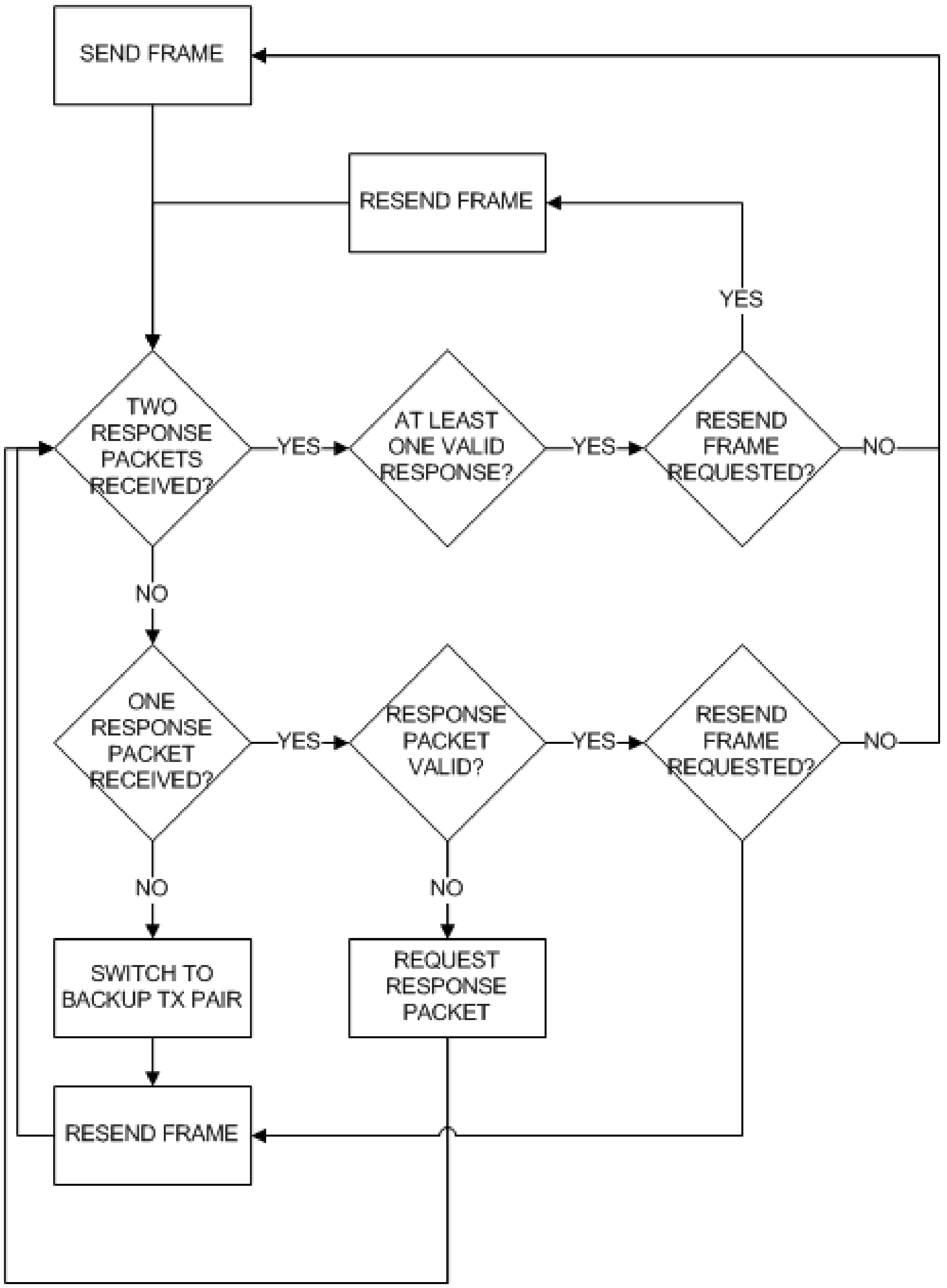
- A serialized example that demonstrates an ARQ
- Ethernet packets by definition include a 32 bit CRC check also called a FCS
- Multiple physical links are required to account for damages wires
- Each data packet an acknowledgement packet

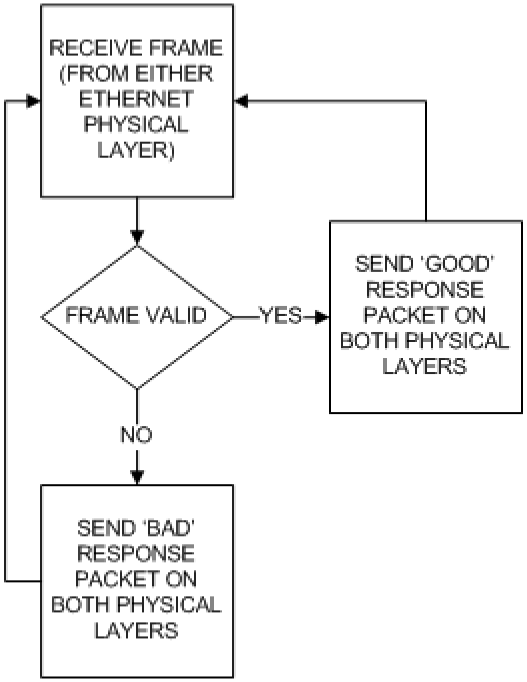
  If the receiver encounters a bad FCS then it requests a resend of the last data packet

  If no response packet is received by the transmitter then serial wires (TX or RX) must be damaged. The system switches to a backup physical link.



Solution Strategies – Ethernet ARQ




RECEIVE FRAME (FROM EITHER ETHERNET PHYSICAL LAYER)
FRAME VALID
YES
SEND 'GOOD' RESPONSE PACKET ON BOTH PHYSICAL LAYERS
NO
SEND 'BAD' RESPONSE PACKET ON BOTH PHYSICAL LAYERS

Advantages and Disadvantages to each Strategy

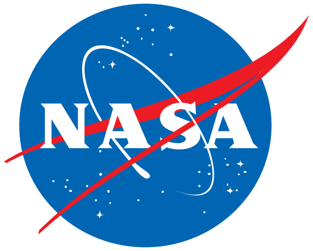
Technology		Channel Efficency		Mass	
Parallel	FEC	Average	Generally speaking the channel efficiency (data_bits/total_bits_with_error_detection) of FECs increase with the number of data bits used. In the case of Hamming codes 8 data bits require 4 parity bits. In this case the channel efficiency is 67%	Average	The mass is a function of the channel effiency. Parallel FEC systems have less mass than TMR systems and fair well with ARQ systems as the number of data wires increases
	TMR	Poor	The channel effiency of any TMR system is 33%.	Poor	
	ARQ	Good	As with hamming codes the channel efficiency increases with the number of data bits. Assuming one spare wire the channel efficiency of a system with 8 data bits is 73%	Good	
Serial	TMR	Good	The channel efficiency of serial system is a measure on how well the system utilizes the link (data_time/total_time). Assuming an ethernet system the channel efficiency is 98%	Average	The mass of a TMR system is always higher than an ARQ system with one spare link
	ARQ	Average	Since a response packet (assuming a minimum size packet) is required for each data packet under the best conditions the channel efficiency is around 94%	Good	

Advantages and Disadvantages to each Strategy

Technology		Latency		Range	
Parallel	FEC	Low	Since FEC systems detect and correct errors without interaction from the source or sink the latency is low	Low	All parallel systems suffer from intersymbol interference, noise, and transmission line properties
	TMR	Low		Low	
	ARQ	High	The additional command and response protocol increases the latency of by at least a factor of two when compared to FEC designs	Low	
Serial	TMR	Low	Since the receiver votes on the content of three packets and does not need to send an acknowledgment packet the latency is low	High	Serial technology has the ability to propagate efficiency over considerably longer cable lengths
	ARQ	High	The data and response packet protocol increases the latency	High	

Suggested Applications

Technology		**Application**
Parallel	FEC	Communication within the same Printed Circuit Board (PCB)
	TMR	
	ARQ	
Serial	TMR	Long range communication where mass is not a concern and the most bandwidth is needed
	ARQ	Long range communication where low mass is required


NASA