DesignCon 2005

Track 5: Chip and Board Interconnect Design (5-WA1)

Performance Model for Inter-chip Busses Considering Bandwidth and Cost

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Problem Statement

- **Performance in VLSI Systems is Limited by Noise from the Package**
- **An Analytical Model for System Performance is needed for:**

1) CAD/CAE

2) Quick Hand Calculations

Agenda

1) Problem Motivation

2) Analytical Model Development

3) Simulation Results

4) Example Use Model

Problem : Packaging Limits Performance

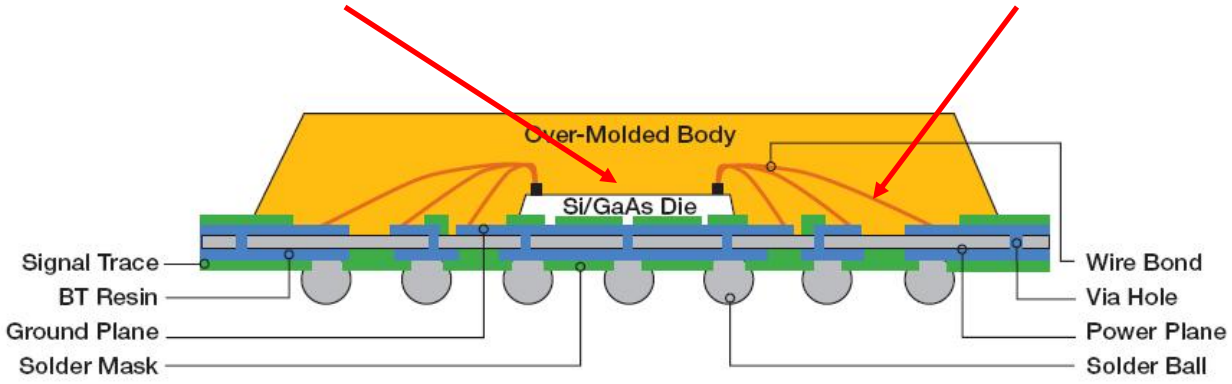
- **Transistor Technology is Faster than Package Technology**

IC

"Moore's Law"
- # of transistors will double every 18 months

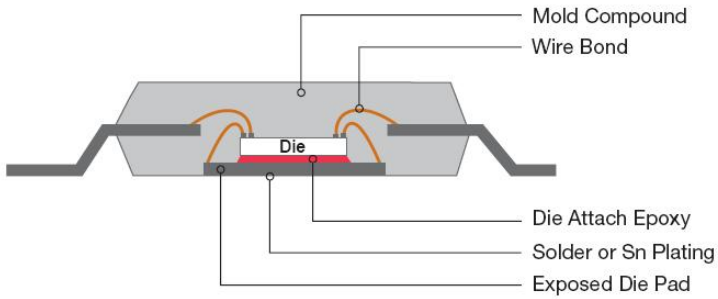
Package

"Rent's Rule"
- # of I/O will double in next 10 years

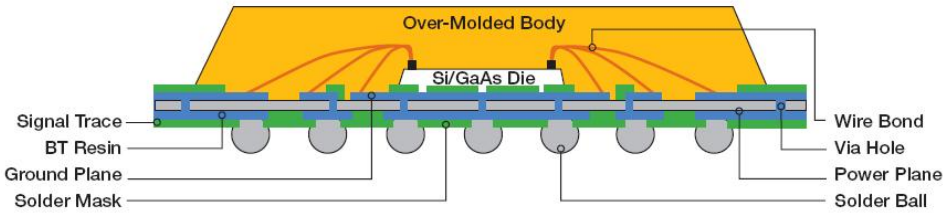


Problem : Packaging Limits Performance

- **Today's Packages Have *Inductive* Parasitics**



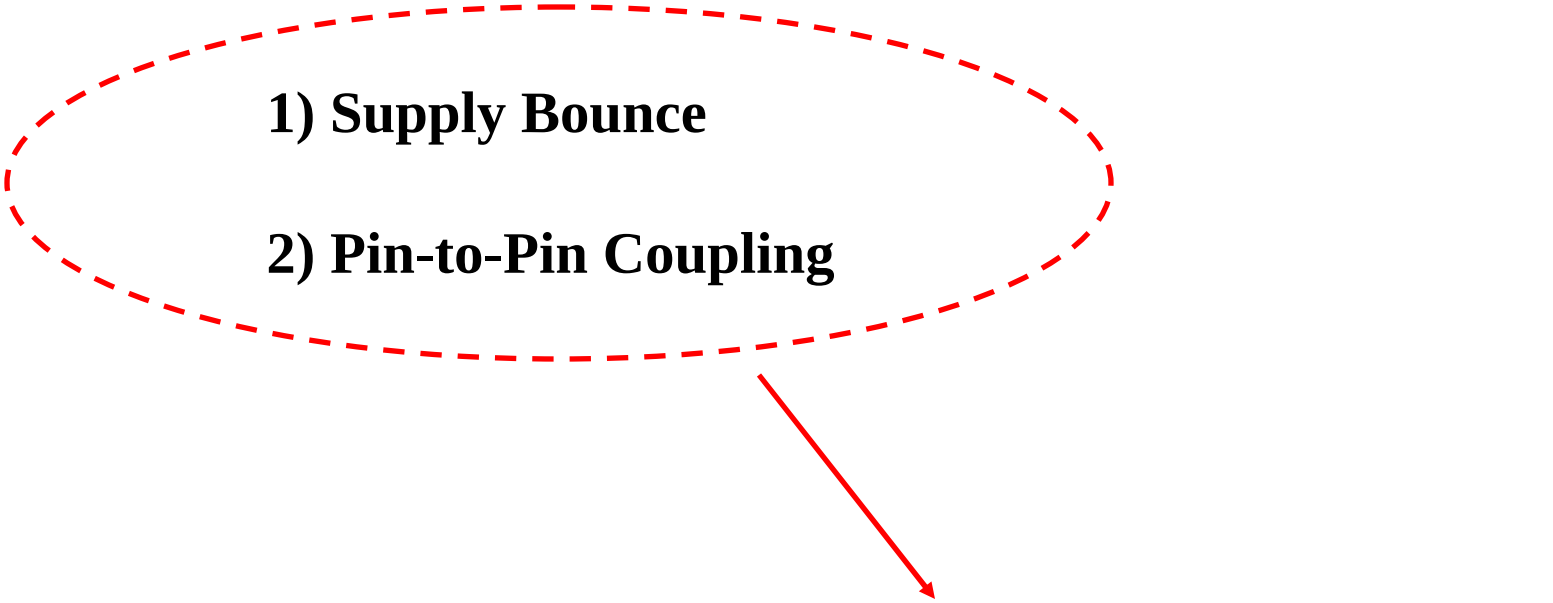
QFP – Wire Bond (~4.5nH)



BGA – Wire Bond (~3.7nH)

Problem : Packaging Limits Performance

- **Inductive Interconnect Causes Noise When Signals Switch:**



Problem : Packaging Limits Performance

1) Supply Bounce

- **Switching current through inductive packaging induces voltage:**

$$V_{bnc} = L \cdot \left(\frac{di}{dt} \right)$$

L = Inductance of pwr/gnd pin that current is being switched through.

- **Multiple Signals Switching Increase the Problem:**

$$V_{bnc} = L \cdot \sum_{i}^{n} \left(\frac{di}{dt} \right)$$

n = # of drivers sharing the power/gnd pin (L).

Problem : Packaging Limits Performance

2) Pin-to-Pin Coupling

- **Switching Signals Couple Voltage onto Neighbors:**

$$V_{couple} = M_{1k} \cdot \left(\frac{di_k}{dt} \right)$$

M = Mutual Inductance between package interconnects.

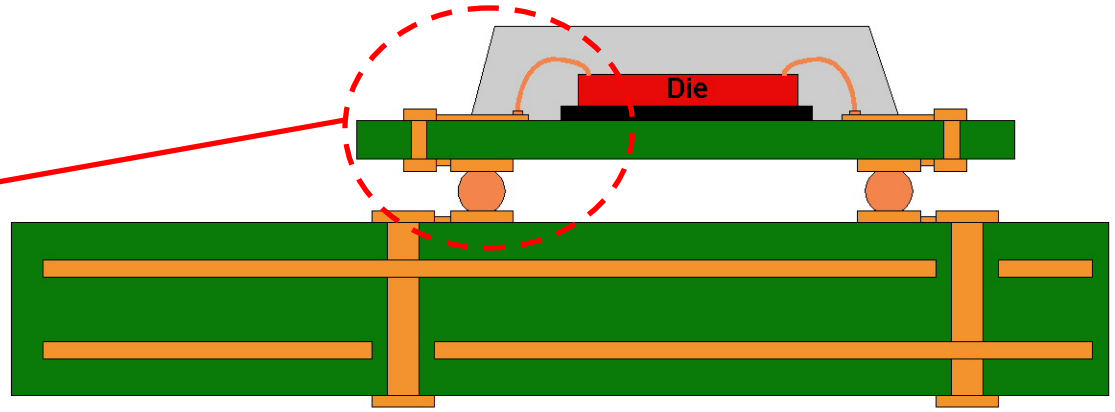
- **Multiple Signals Switching Increase the Problem:**

$$V_{couple} = \sum_{1}^{k} M_{1k} \cdot \left(\frac{di_k}{dt} \right)$$

Problem : Packaging Limits Performance

- **Package Inductance Creates *Simultaneous Switching Noise***

SSN

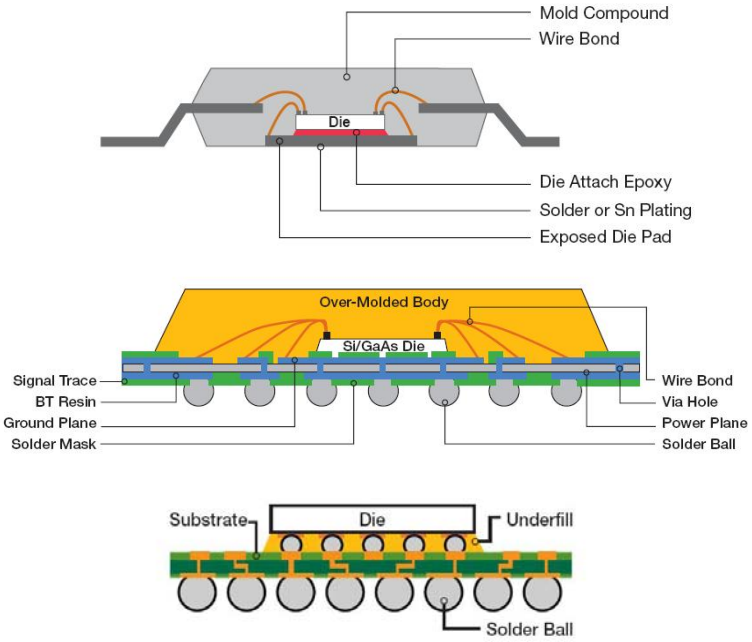


- **SSN in Package Limits di/di**

$$\frac{di}{dt} \propto SSN$$

Problem : Packaging Limits Performance

- **Aggressive Package Design will Reduce Inductance**



QFP – Wire Bond : 4.5nH → $0.22 / pin

BGA – Wire Bond : 3.7nH → $0.34 / pin

BGA – Flip-Chip : 1.2nH → $0.63 / pin

- **But is Expensive**

- 95% of VLSI design-starts are wire-bond

Problem : Packaging Limits Performance

- **Modern Design Practice**

  1) Acceptable SSN Limits are Defined.
  2) Fastest (di/dt) is selected that doesn't violate limits.

- **Limitations of Approach**

  - **SPICE is used to evaluate SSN.**
  - **This takes too much time.**
  - **The entire range of variables cannot be evaluated quickly (package, # of pwr/gnd, bus width, etc…).**

Problem : Packaging Limits Performance

- **We need an *Analytical Model* to Evaluate Off-Chip Bus Performance**

  1) Package Parasitics
  2) Package Cost
  3) Bus Width
  4) # of Power/Grounds

- **This can be used to find Optimal Bus Configuration**

”Desired Performance for the Least Cost”

Analytical Model

- **Test Circuit Topology**

- 0.1um CMOS Tx/Rx

- +1.5v V_{DD}, 0.35 Vt

- 25mA Drive Strength

- Series Terminated

Analytical Model

- **Failure Modes**

Power Supply Droop

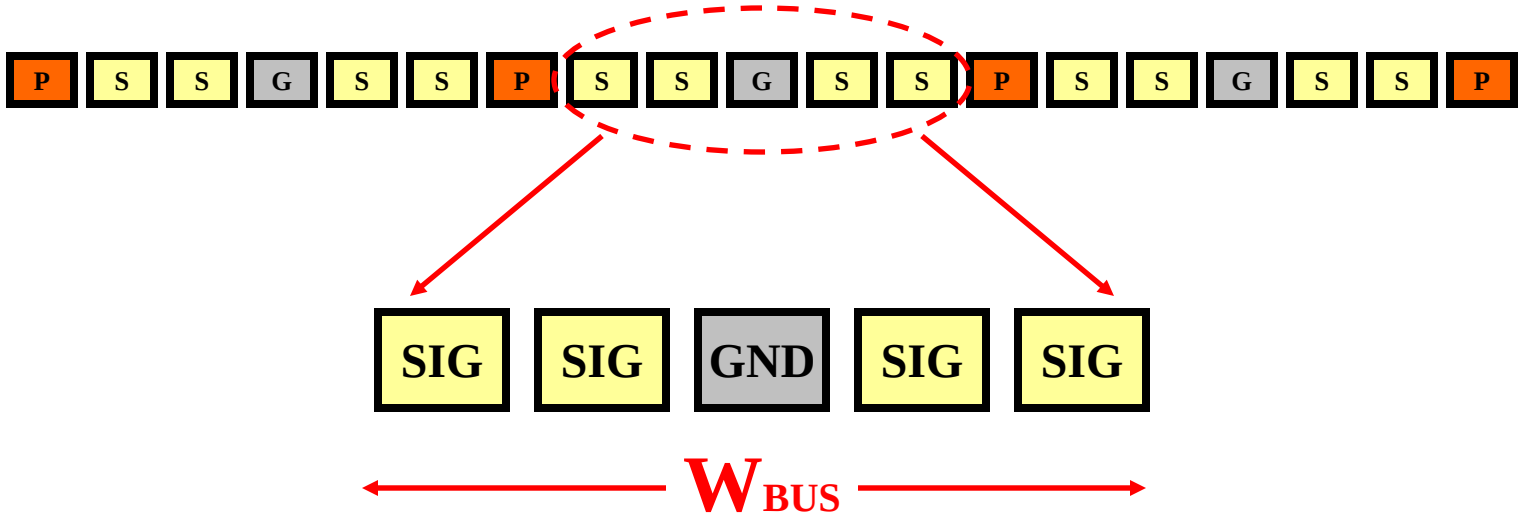
Signal Coupling

Ground Bounce

Power Supply Droop = Ground Bounce

Analytical Model

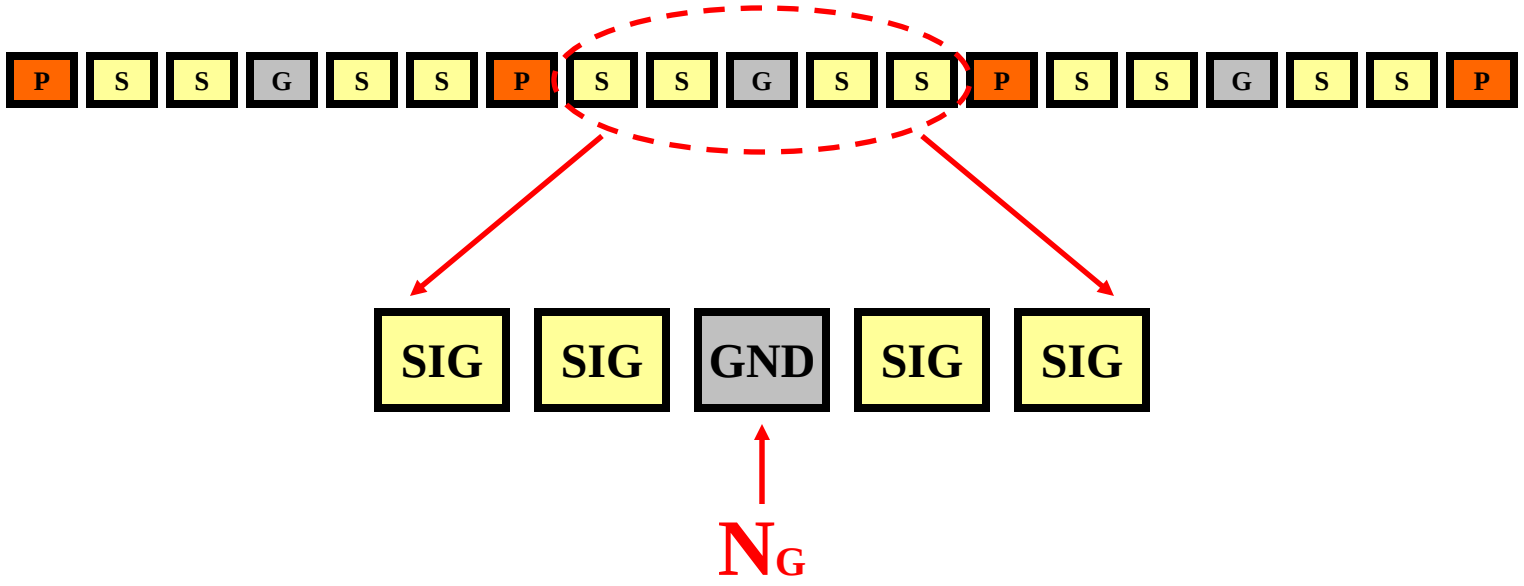
- **Bus Parameters**



W_{BUS} : # of Signals Per Bus Segment of Interest

Analytical Model

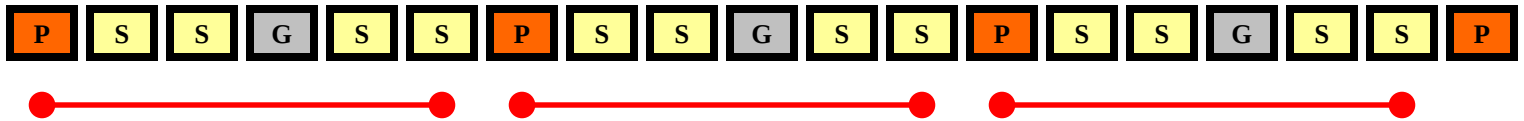
- **Bus Parameters**



N_G : # of Grounds Per Bus Segment of Interest

Analytical Model

- **Bus Parameters**



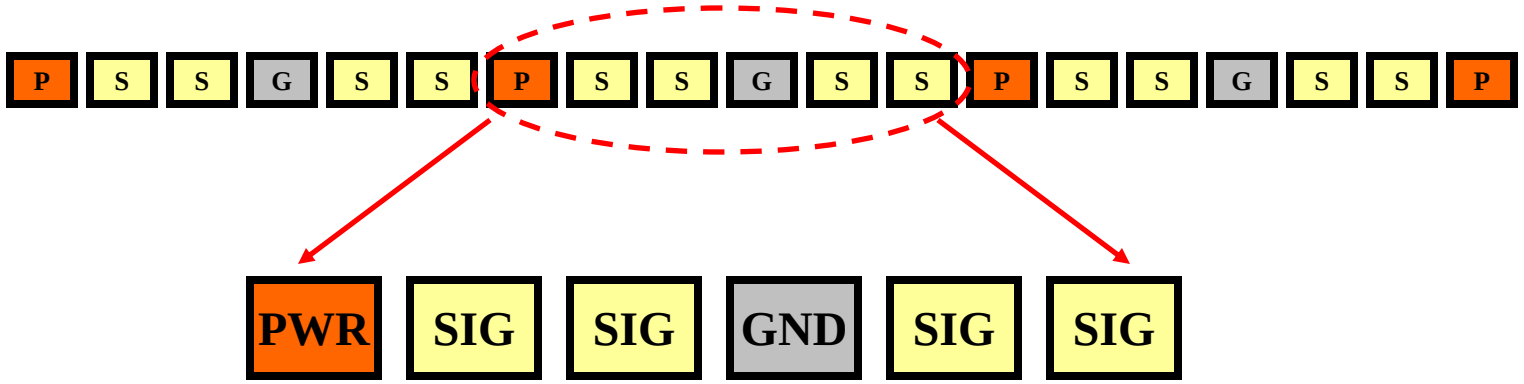
Repetitive Pattern of Signal, Power, and Ground Pins

SPG : (# of Signals) : (# of PWR's) : (# of GND's)

SPR : SPG Ratio

Analytical Model

- **Bus Parameters**



Example:

W_{BUS} : 4

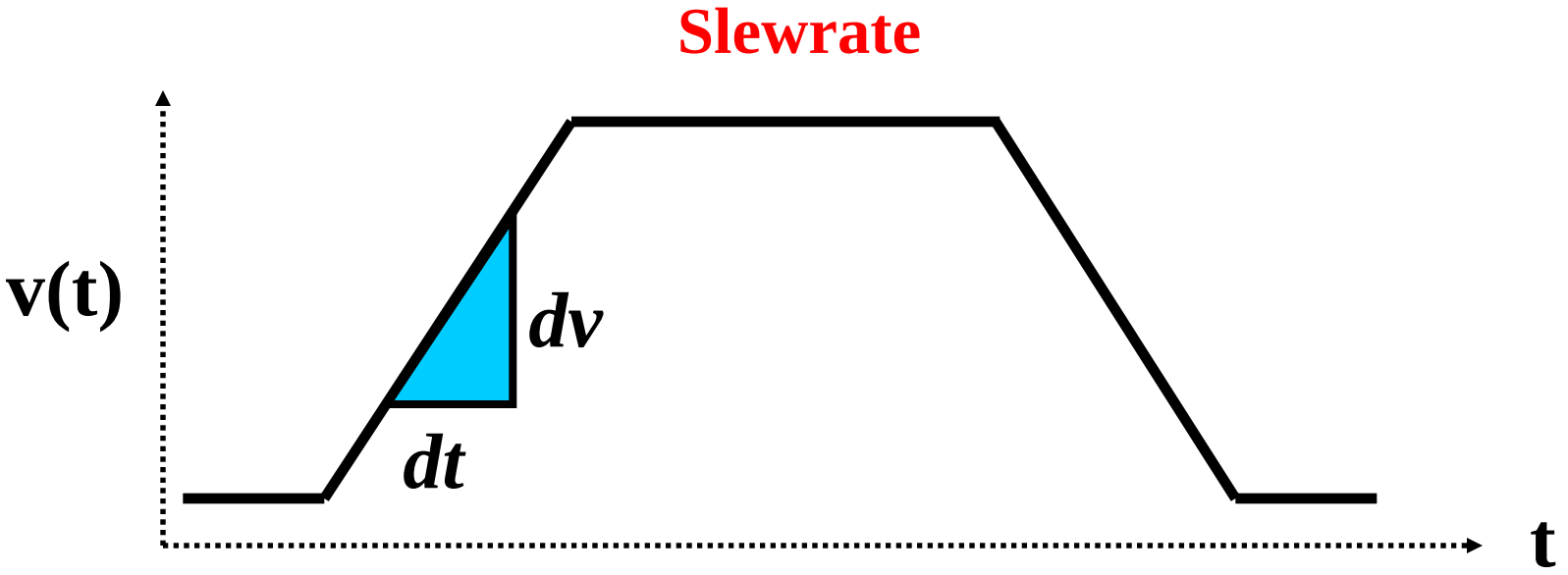
N_G : 1

SPG : 4:1:1

SPR : 4

Analytical Model

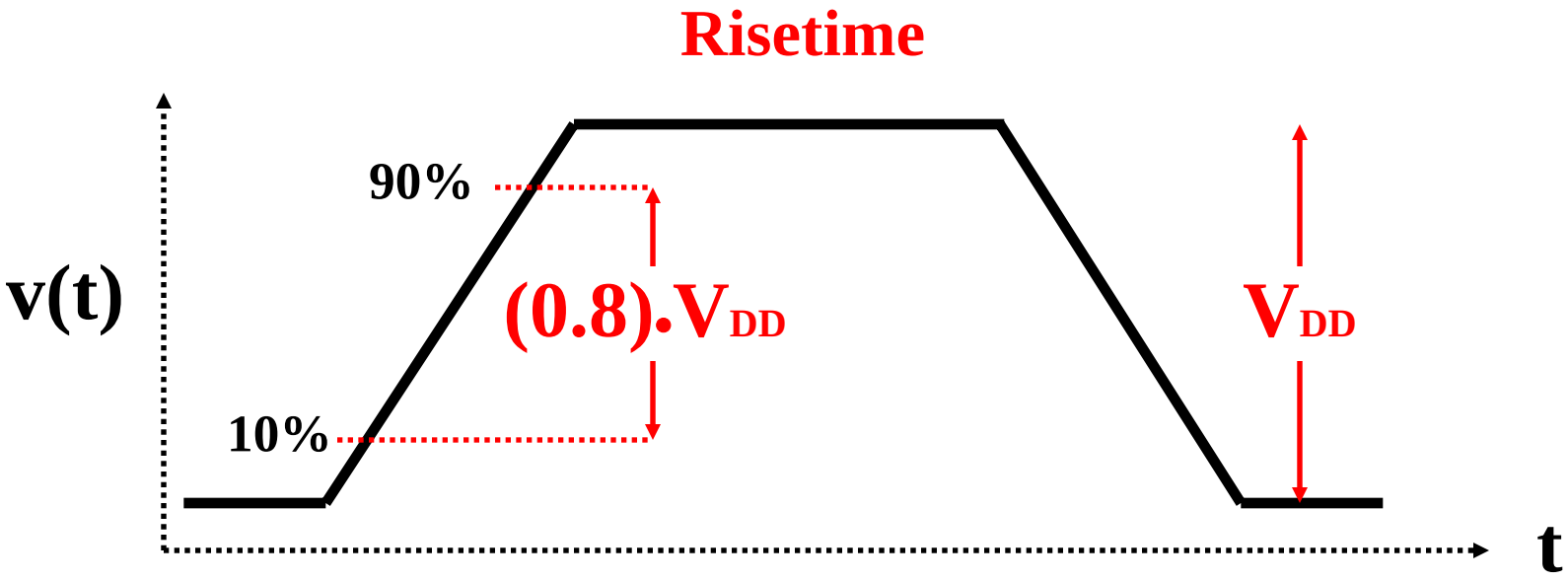
- **Bus Performance Description**



$$slewrate = \left(\frac{dv}{dt}\right) = \left(\frac{di}{dt}\right) \cdot Z_{load}$$

Analytical Model

- **Bus Performance Description**

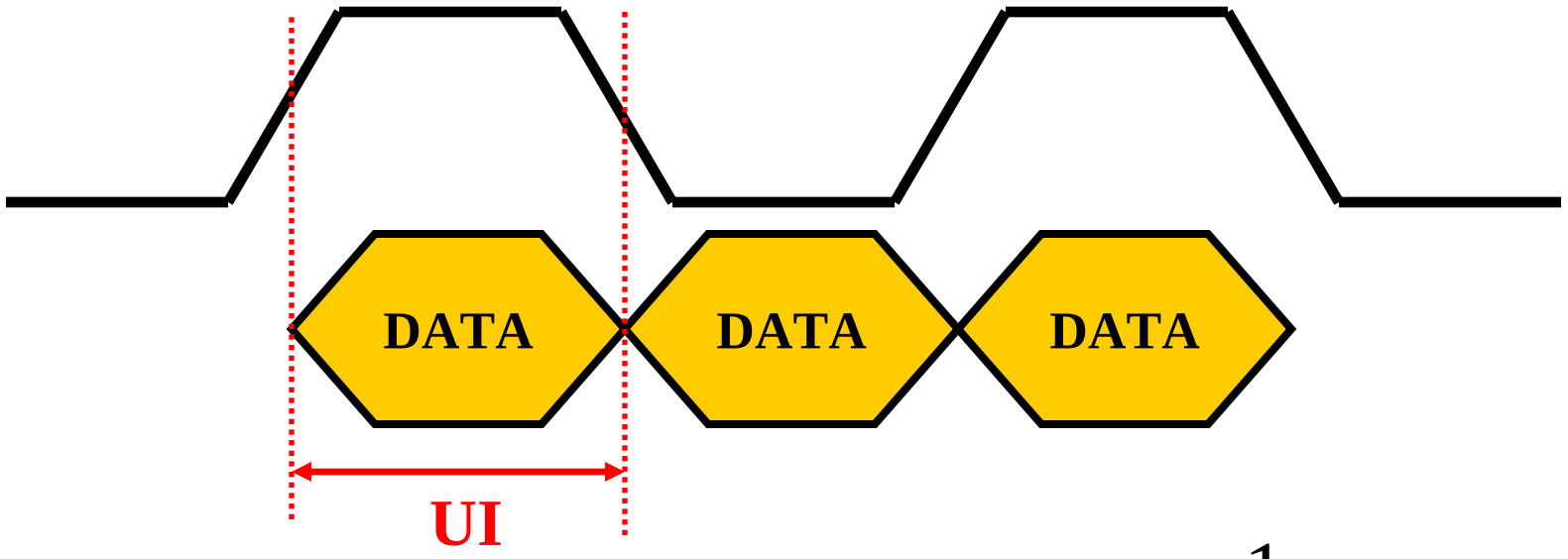


$$t_{rise} = \frac{(0.8) \cdot V_{DD}}{slewrate}$$

Analytical Model

- **Bus Performance Description**

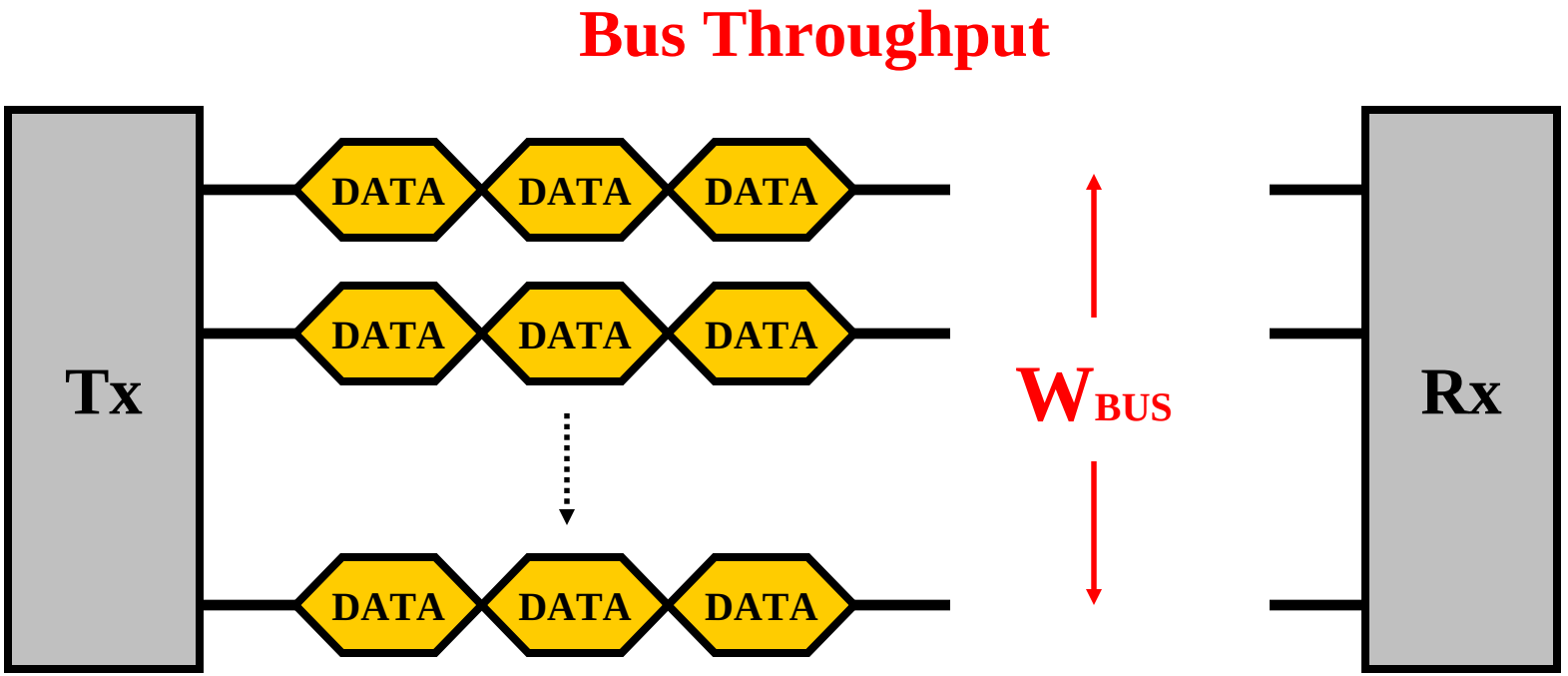
Minimum Unit Interval



$$UI_{\min} = (1.5) \cdot t_{rise} = \frac{1}{DR_{\max}}$$

Analytical Model

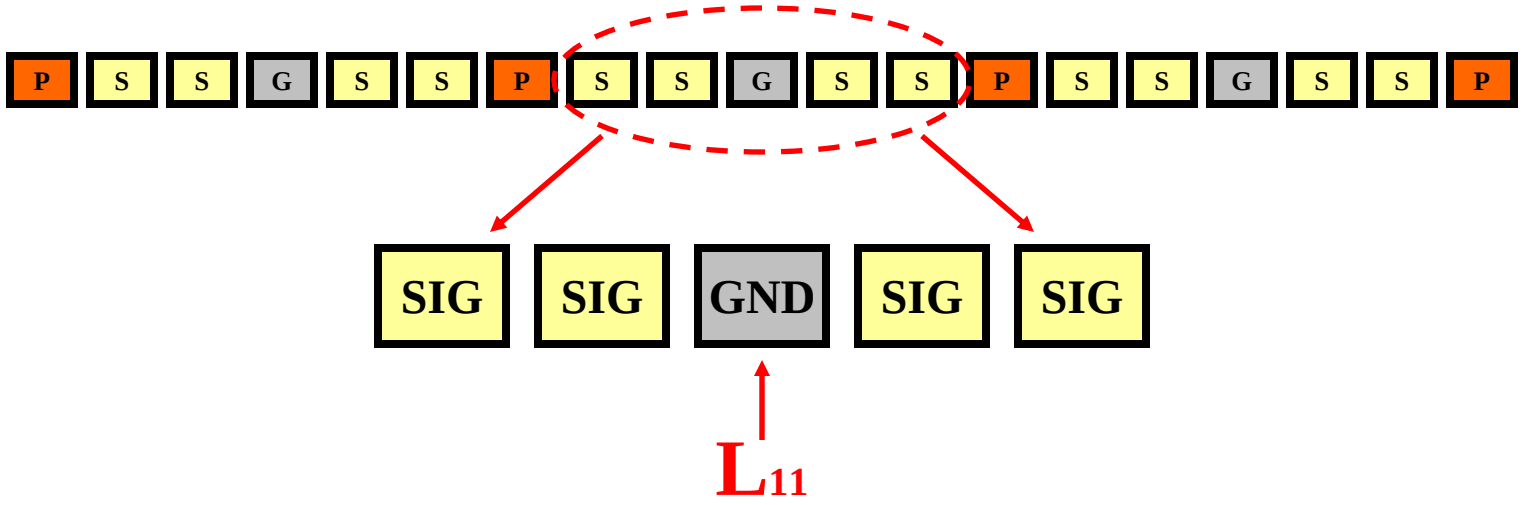
- **Bus Performance Description**



$$TP_{\max} = W_{BUS} \cdot DR_{\max}$$

Analytical Model

- **Bus Performance Limits**

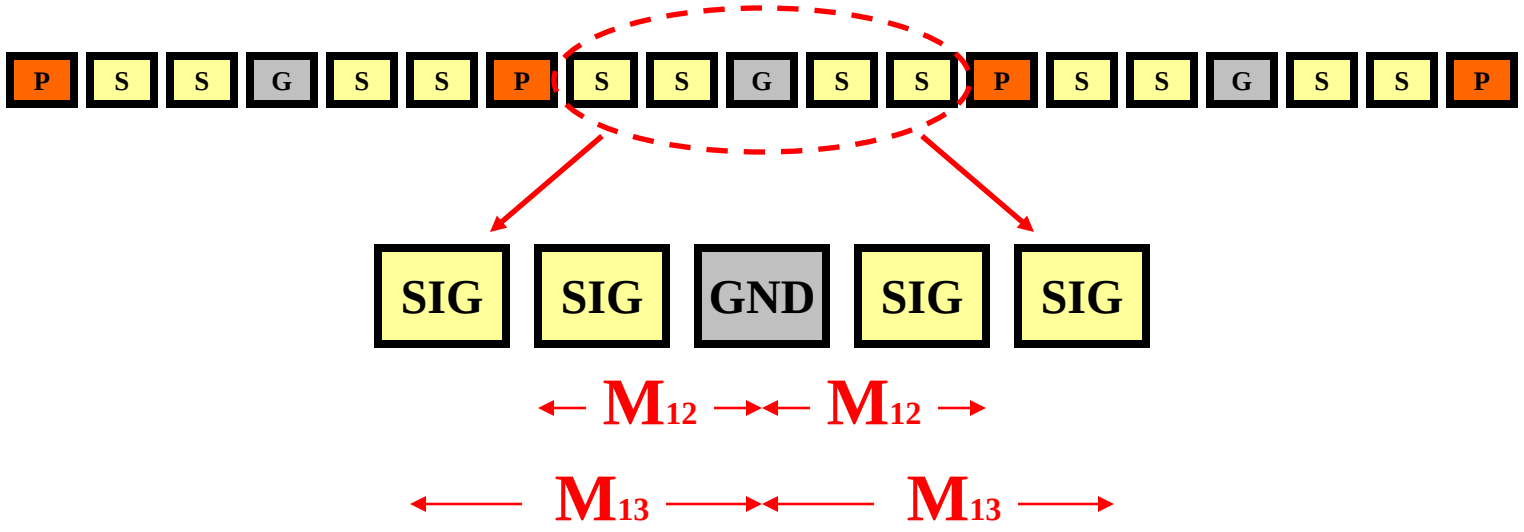


L_{11} : Self Inductance of Ground Path

$$V_{bnc_{self}} = L_{11} \cdot \sum_{1}^{W_{bus}} \left(\frac{di_1}{dt} \right)$$

Analytical Model

- **Bus Performance Limits**



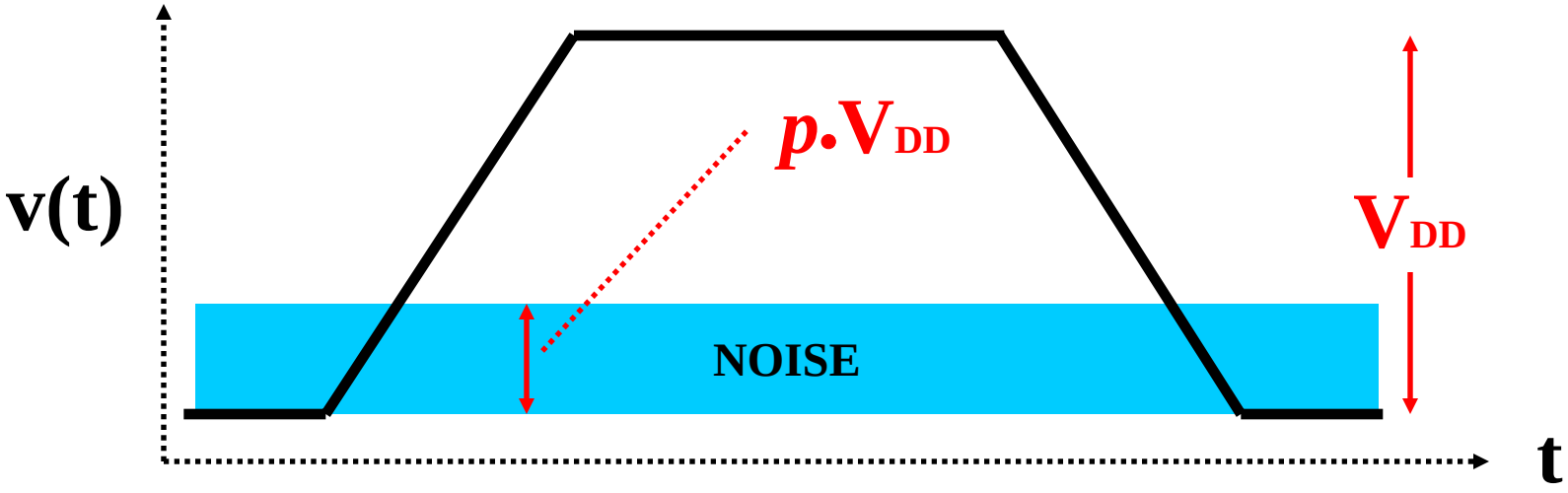
M_{1k} : Mutual Inductance Between Pins

$$V_{bnc_{couple}} = \sum_{2}^{W_{bus}} M_{1k} \cdot \left(\frac{di_k}{dt} \right)$$

Analytical Model

- **Bus Performance Limits**

Maximum Acceptable Ground Bounce



$$V_{bnc-MAX} = p \cdot V_{DD}$$

($p_{typical}$ = 5%)

Analytical Model

- **Model Development**

Maximum Ground Bounce

$$V_{gnd-bnc} = p \cdot V_{DD} = \left(\frac{W_{bus} \cdot L_{11}}{N_g} \right) \left(\frac{di}{dt} \right) + \sum_{k=2}^{W_{bus}} \left(M_{1k} \frac{di}{dt} \right)$$

Self Contribution ***Coupling Contribution***

Analytical Model

- **Model Development**

Maximum Slewrate

$$\left(\frac{dv}{dt}\right)_{\max} = \frac{p \cdot V_{DD} \cdot Z_{load}}{\left(\frac{W_{bus} \cdot L_{11}}{N_g}\right) + \sum_{k=2}^{W_{bus}} M_{1k}}$$

- pull out (di/dt)

- convert to (dv/dt)

Analytical Model

- **Model Development**

Minimum Risetime

$$t_{rise-\min} = \frac{(0.8)\cdot\left[\left(\frac{W_{bus}\cdot L_{11}}{N_g}\right)+\sum_{k=2}^{W_{bus}}\left(M_{1k}\right)\right]}{p\cdot Z_{load}}$$

- convert slewrate to risetime

Analytical Model

- **Model Development**

Maximum Datarate

$$DR_{\max} = \frac{p \cdot Z_{load}}{(1.5)\cdot(0.8)\cdot\left[\left(\frac{W_{bus}\cdot L_{11}}{N_g}\right) + \sum_{k=2}^{W_{bus}} M_{1k}\right]}$$

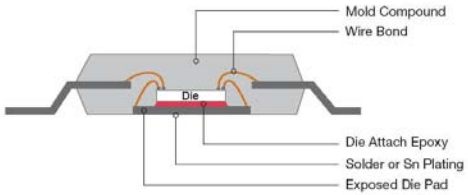
- convert Risetime to Datarate

Maximum Throughput

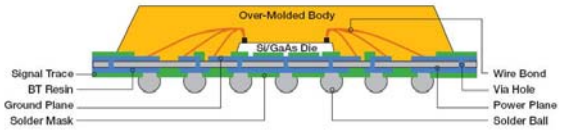
$$TP_{\max} = W_{BUS} \cdot DR_{\max}$$

Experimental Results

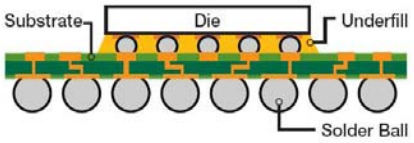
- **SPICE Simulations were Performed on Three Packages**



QFP – Wire Bond



BGA – Wire Bond



BGA – Flip-Chip

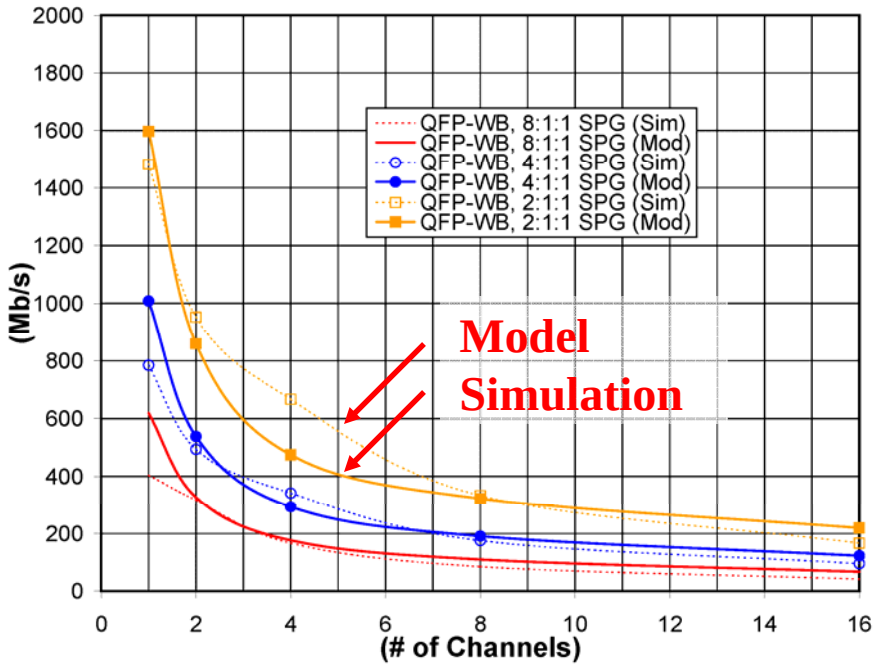
Package	L_{11}	K_{12}	K_{13}	K_{14}	K_{15}	K_{16}
QFP-wb	4.550n	0.744	0.477	0.352	0.283	0.263
BGA-wb	3.766n	0.537	0.169	0.123	0.097	0.078
BGA-fc	1.244n	0.630	0.287	0.230	0.200	0.175

Package	Cost Per-Pin
QFP-wb	$0.22
BGA-wb	$0.34
BGA-fc	$0.63

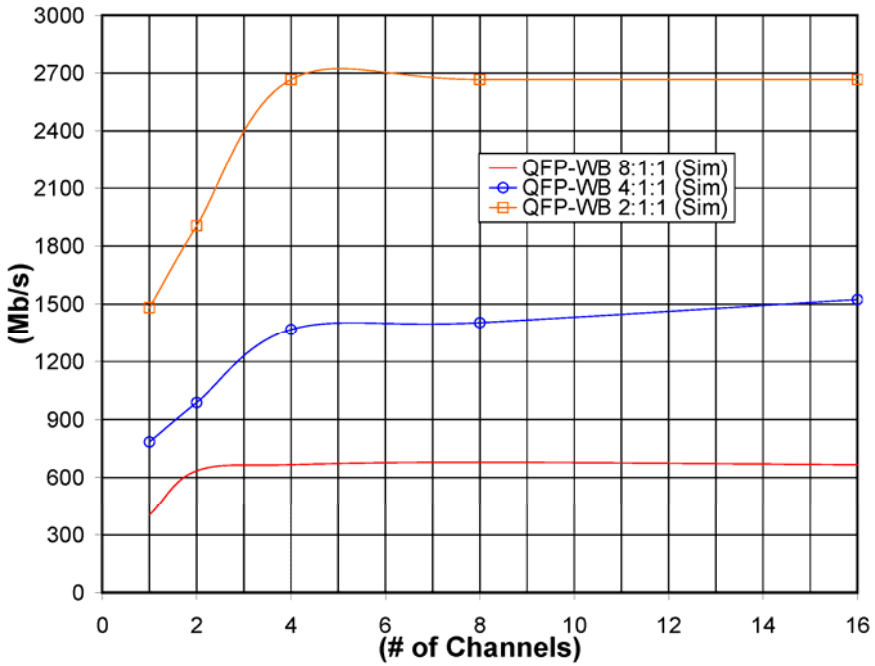
Experimental Results

- **QFP Wire-Bond Package Simulations**

Per-Pin Data-Rate



Bus Throughput

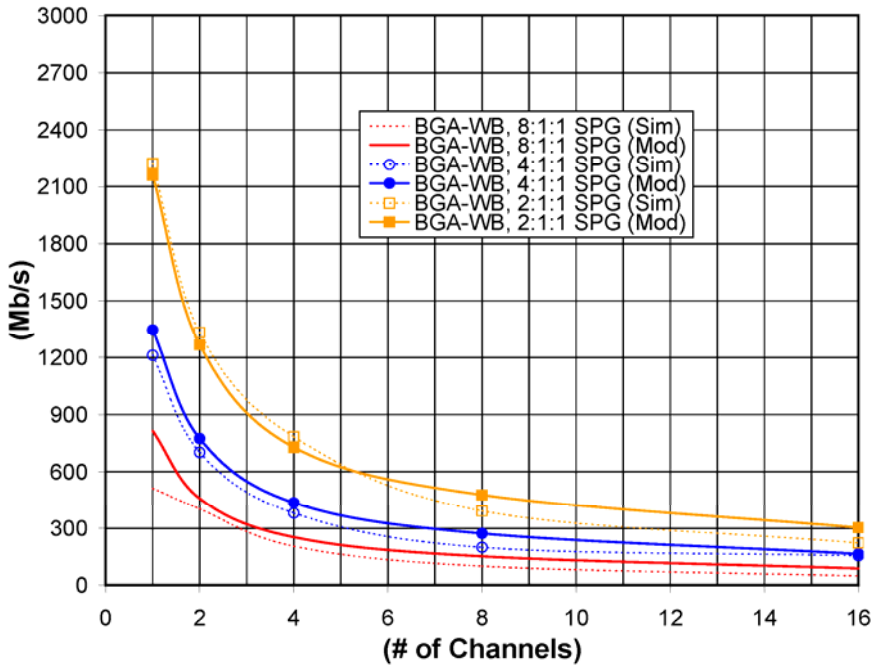


- Throughput reaches an asymptotic limit as channels are added

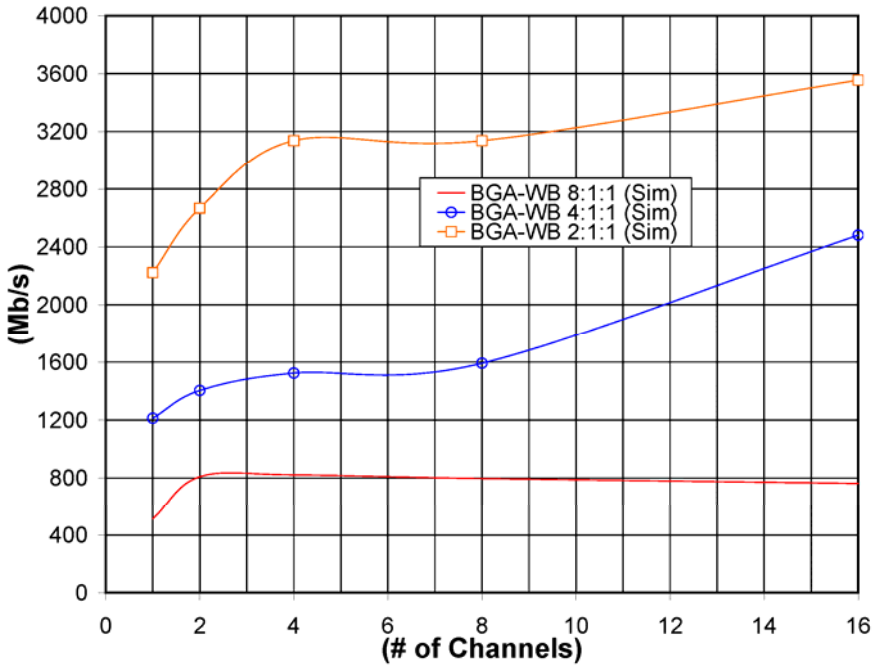
Experimental Results

- **BGA Wire-Bond Package Simulations**

Per-Pin Data-Rate



Bus Throughput

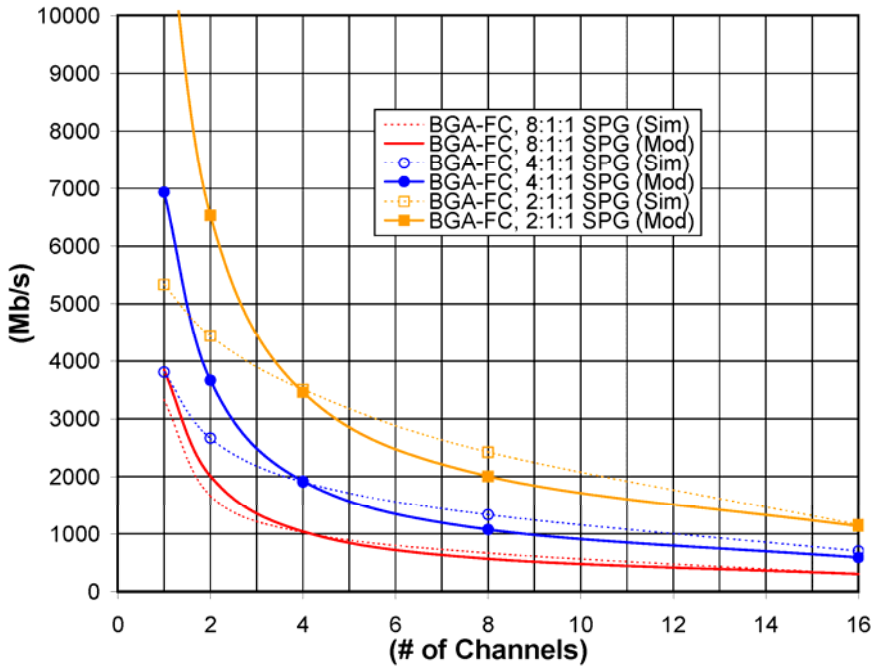


- Level 1 : BGA Increases Performance Over QFP

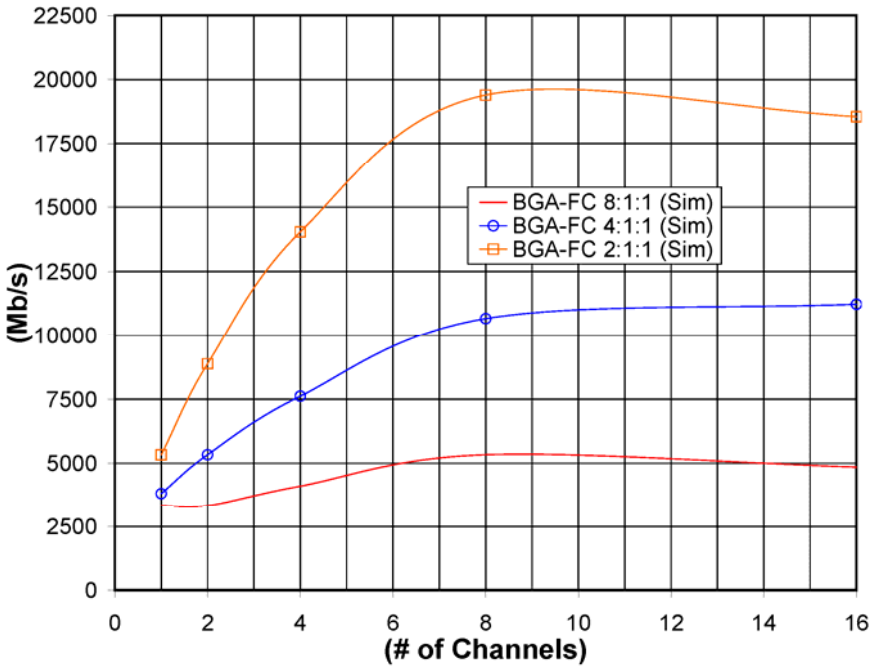
Experimental Results

- **BGA Flip-Chip Package Simulations**

Per-Pin Data-Rate



Bus Throughput



- Level 2: Flip-Chip Increases Performance Over Wire-Bond

Experimental Results

- **Cost Must Also Be Considered in Analysis**

Bandwidth Per Cost

$$BPC = \left(\frac{TP}{Cost_{bus} \cdot 1e^{6}} \right)$$

Units = (Mb/$)

- **This Metric Represents *"Cost Effectiveness of the Bus"***

Experimental Results

- ***Cost* per Bus Configuration**

$

Bus Configuration	Number of Channels				
	1	2	4	8	16
QFP-WB 8:1:1	0.66	0.88	1.32	2.20	4.40
QFP-WB 4:1:1	0.66	0.88	1.32	2.62	5.28
QFP-WB 2:1:1	0.66	0.88	1.76	3.52	7.04
BGA-WB 8:1:1	1.02	1.36	2.04	3.40	6.80
BGA-WB 4:1:1	1.02	1.36	2.04	4.08	8.16
BGA-WB 2:1:1	1.02	1.36	2.72	5.44	10.88
BGA-FC 8:1:1	1.89	2.52	3.78	6.30	12.60
BGA-FC 4:1:1	1.89	2.52	3.78	7.56	15.12
BGA-FC 2:1:1	1.89	2.52	5.04	10.08	20.16

- **Performance Increases with Cost *(Package, SPG)***

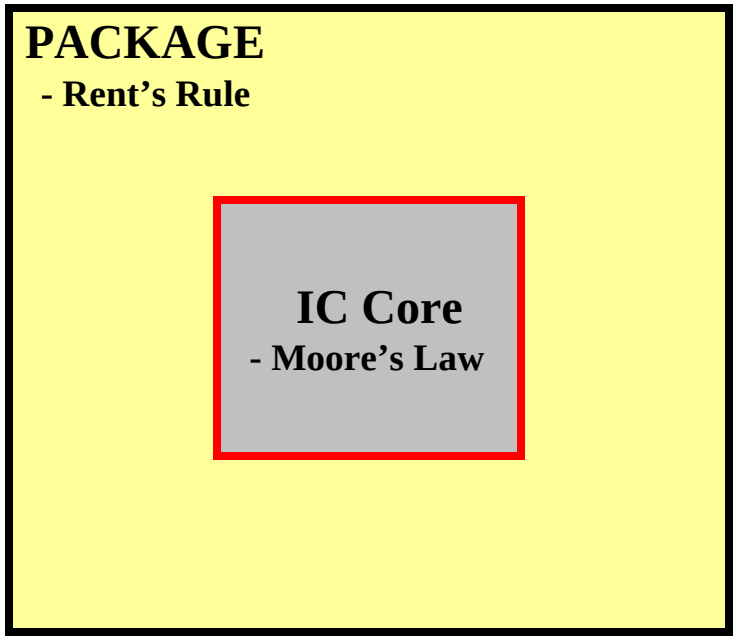
Experimental Results

- ***Bandwidth Per Cost* Results**

Bus Configuration	Number of Channels				
	1	2	4	8	16
QFP-WB 8:1:1	612	722	505	309	152
QFP-WB 4:1:1	1188	1122	1036	532	289
QFP-WB 2:1:1	2245	2165	1515	758	379
BGA-WB 8:1:1	503	594	402	234	112
BGA-WB 4:1:1	1188	1032	747	390	304
BGA-WB 2:1:1	2179	1961	1153	577	327
BGA-FC 8:1:1	1764	1323	1085	847	385
BGA-FC 4:1:1	2016	2116	2016	1411	743
BGA-FC 2:1:1	2822	3527	2785	1924	920

Faster Narrower Busses = More Cost Effective

Example



On-Chip

- 8 bit Data Bus
- 300 Mb/s

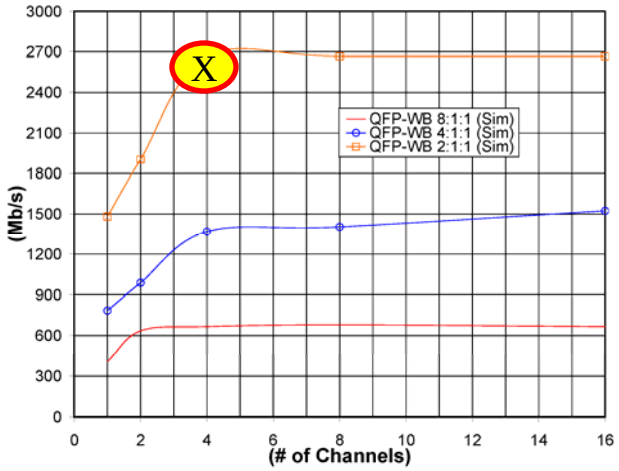
Package

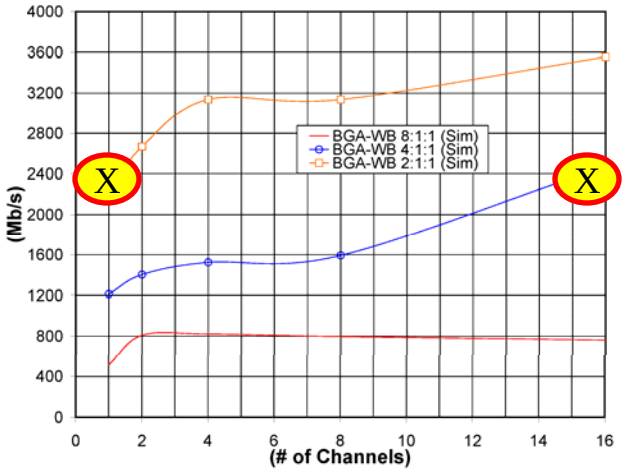
- Need

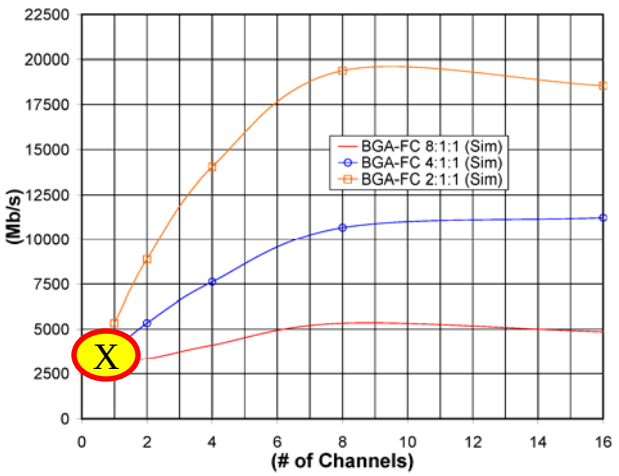
(8)(300M) = **2400 Mb/s**

Example

Need: **2400 Mb/s**







QFP – Wire Bond

- 4 bits wide, SPG=2:1:1

BGA – Wire Bond

- 1 bit wide, SPG=2:1:1
- 16 bits wide, SPG=4:1:1

BGA – Flip-Chip

- 1 bit wide, SPG=2:1:1
- 1 bit wide, SPG=4:1:1
- 1 bit wide, SPG=8:1:1

Example

- **Cost of Each Bus Configuration**

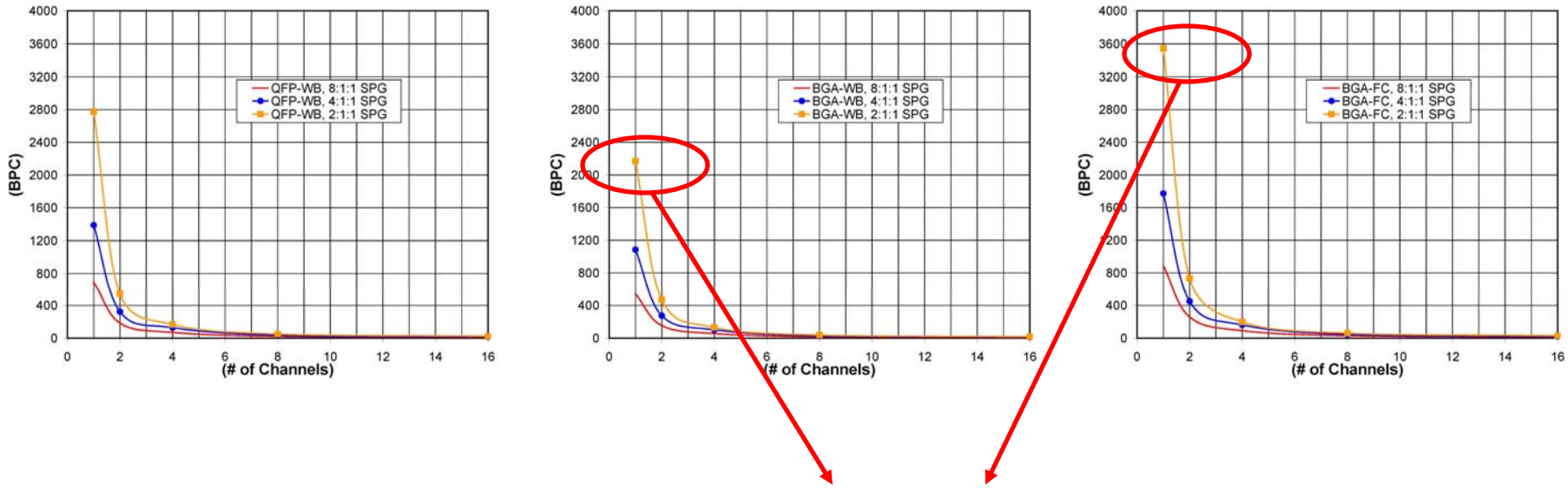
Bus Configuration	Number of Channels				
	1	2	4	8	16
QFP-WB 8:1:1	0.66	0.88	1.32	2.20	4.40
QFP-WB 4:1:1	0.66	0.88	1.32	2.62	5.28
QFP-WB 2:1:1	0.66	0.88	1.76	3.52	7.04
BGA-WB 8:1:1	1.02	1.36	2.04	3.40	6.80
BGA-WB 4:1:1	1.02	1.36	2.04	4.08	8.16
BGA-WB 2:1:1	1.02	1.36	2.72	5.44	10.88
BGA-FC 8:1:1	1.89	2.52	3.78	6.30	12.60
BGA-FC 4:1:1	1.89	2.52	3.78	7.56	15.12
BGA-FC 2:1:1	1.89	2.52	5.04	10.08	20.16

Most Cost Effective:

- BGA-WB
- W_{bus} = 1
- SPG = 2:1:1

Example

- **Bandwidth-per-Cost of Each Bus Configuration**



Higher BPC = More Headroom

Summary

1) **Package Noise Limits System VLSI Performance**

2) **An Analytical Model was Presented to Predict Bus Performance**

3) **Datarate Approaches an Asymptotic Limit as Channels are Added**

4) **Throughput Can be Achieved Using Different Bus Configurations**

Questions?