# Off-Chip Coaxial to Microstrip Transition Using MEMs Trench

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***Abstract*- This paper will report the initial investigation into creating an off-chip coaxial launch for use in improving data throughput in System-on-Package applications. This type of launch will reduce the simultaneous switching noise (SSN) associated with getting high speed signals on and off of CMOS processing substrates using traditional packaging techniques. This launch will consist of a trench formed on the CMOS substrate that acts as a transition point for a miniature coaxial interconnect. The trench will be formed using MEMs processing techniques targeted at a Silicon substrate. The trench will be plated to make contact with the coaxial ground shield forming a low loss return path. This return path will considerably reduce SSN and enable much higher off-chip data rates. If successful, this new type of interconnect will decrease the bottleneck of transmitting large amounts of information off-chip and present a major breakthrough for System on Package performance.**

## I. Introduction

On-chip digital system performance is increasing at an exponential rate due to advances in integrated circuit fabrication processes. The on-chip data rates are already outpacing the capability of off-chip transmission systems. This imbalance in performance is causing a bottleneck in the computational power of modern systems and will only be exacerbated as IC feature sizes continue to shrink into the deep submicron region. In addition, the computational power of CMOS processors cannot be fully exploited if signals cannot be adequately transmitted onto the Silicon substrate.

The main limitation of getting signals on and off chip is due to the physical interconnect that connects the IC substrate to the system substrate [1,2]. Traditional off-chip interconnect has been designed primarily for mechanical reasons such as reliability and manufacturability. This was acceptable when the on-chip performance limited the overall system performance. However, with the increase of on-chip performance in the past few years, systems are now left with legacy package interconnect which is now the leading limitation to system capability.

The package interconnect limits overall performance due to the noise that is induced into the system from the parasitic inductance and capacitance of the interconnect [1,2,3]. These parasitics lead to simultaneous switching noise, power supply droop, and impedance discontinuities. Each of these noise sources limits the ability to transmit signals on/off chip and hence dampers the potential for exploiting the computational power of CMOS processing.

Today's package interconnect consists of unshielded conductors (wirebonds, flip-chips, leadframes, BGAs) placed in an array or perimeter fashion on the IC substrate (figure 1), [4]. These interconnects have two major drawbacks. The first is that they are orders of magnitude larger than the on-chip interconnect. This causes excess electrical parasitics (L & C) which lead to mismatches in the performance between on and off-chip transient behavior. The second drawback is that the unshielded configuration leads to inductive and capacitive coupling between conductors. This leads to unwanted noise on signal lines which can cause unwanted switching of digital circuits or insertion loss due to reflections when transmitting analog signals.

Off-chip SSN is a critical problem in System-on-Package (SoP) applications. One such application is the interface between a microprocessor and memory configured as two independent chips on a single package substrate. This type of configuration decreases the physical size of the total interconnect because the connection is only made to the package. This approach has the advantage of using smaller interconnect, which has less parasitic inductance and capacitance. It also attempts to exploit the cost advantages of design segmentation. This type of system is still limited by the overall interconnect because the same mechanical connections are used as in the chip-to-board connection, albeit at a smaller scale.

Another SoP application that suffers from off-chip interconnect deficiencies is the integration of CMOS processing and wireless communication. SoP has the inherent advantage that different circuit substrates can be used in a single package. This allows the optimal material to be chosen for the application. Silicon has long been the material of choice for Digital CMOS circuitry due to its low static power consumption. However, when interfacing to a wireless signal, Silicon Germanium (SiGe) tends to be a better material for telecommunications circuits such as amplifiers and mixers which require

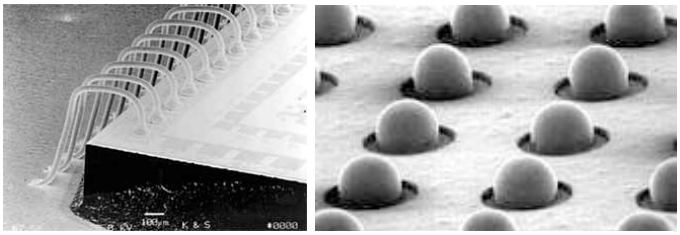

Figure 1. SEM view of current package interconnect technology (Wirebonding on Left, Flip-Chip on Right)

more power. SoP allows application specific materials to be used and interfaced using package interconnect. In this situation, a high quality interconnect is of great importance on the package because the signals are often high frequency and analog in nature. Getting a high quality analog connection between SiGe and Silicon can enable Silicon-based Analog-to-Digital Conversions (ADC) and demodulation via Digital Signal Processing (DSP). This application is being brought to market in the form of Software Controller Radio (SCR). This technology has great promise but will ultimately be limited by the lack of a high speed connection between multiple substrates within the package.

In this paper, we present an initial feasibility study on creating a micro-scale, coaxial to microstrip launch for use as an off-chip interconnect in SoP applications. A Silicon substrate which contains a controlled impedance microstrip trace is processed using Micro Electrical Mechanical (MEM) steps in order to create a plated trench. A miniature coaxial cable with an extended center conductor is placed into the trench such that the ground of the Silicon substrate makes a ground connection with the outer shield of the coaxial cable. The Silicon microstrip trace then makes contact with the extended center conductor of the coax. This type of off-chip interconnect provides shielding for the signal path in addition to a controlled and dedicated path for the return current. This will inherently reduce SSN and enable a higher speed connection between an integrated circuit and package substrates.

## II. Previous Work

### A. Waveguide Transitions

There has been extensive work in modeling and fabricating transitions into and out of waveguides [5,6,7,8]. Typically a wave traveling within a waveguide can be accessed by inserting an antenna at a predetermined wavelength of the traveling signal in order observe the signal with minimal destructive interference. This type of transition is widely accepted for microwave frequencies as a way to convert the transmission medium from air within the waveguide to a metal conductor on the target substrate. In a standard approach, the antenna consists of the exposed center conductor of a coaxial transmission line.

Modifications of the above mentioned approach have been illustrated that lend themselves well to transitioning from a coaxial transmission line to a planar Silicon structure. It has been shown that waveguides can be successfully constructed with novel structures besides the standard rectangular and cylindrical shapes that are typically associated with waveguides. Structures such as *Troughguides* [9] allow the TEM waves to be transmitted and guided in a polygonal shaped cavity as opposed to rectangular.

Also, different coupling mechanizing between the guide and wire line connection have been investigated. In [10,11], the authors report a Ka-band coupler that is based upon a micromachined coaxial structure. Exploring different coupling constructions gives flexibility to designers when constructing an application specific interconnect.

### B. Wire Line Transitions

There has also been work into making high frequency transitions between wire line transmission structures. In [12], the authors report a novel technique to transition millimeter-waves between a coaxial and a microstrip transmission line using a perpendicular connection. The authors of [13] also report a coaxial transition to a planar substrate using a *Quasi Half Coax* line on the IC substrate.

Prior work into improving wire line connections for application to off-chip transitions demonstrates the feasibility of applying micro-machining processes to address the electrical problems of modern package interconnect.

### C. MEMs Cavities

The fundamental principle of micro-machining is to form a desired structure through a series of etch, growth, and release steps [14]. This principle has been applied to a variety of applications. One of the most common applications is a capacitive accelerometer [15]. In this type of construction, a Deep Reactive Ion Etch (DRIE) is used to form a cavity on a Silicon substrate. A Silicon Oxide ($SiO_2$) release layer is then grown on the Silicon to help form the structure and also bond with a subsequent structural layer of Nitride. The Nitride will be able to accept a patterned electrode, typically of polysilicon. A release step is then used to remove the $SiO_2$. The Nitride containing the electrode will remain and yield a suspended electrode over a cavity. The Nitride's structural behavior allows it to move freely above the cavity. Other electrodes are patterned along the edges of the cavity. As the device is accelerated, the freely suspended electrode moves relative to the cavity due to different mass densities. As the electrode moves across the cavity, it gets closer or further from perimeter electrodes which monitor the capacitance between the electrode pairs and thus acceleration.

This process has been improved upon to create optical devices such as micro mirrors [16,17]. By patterning flat surfaces that are molded by the Silicon Nitride, freely suspected mirrors can be created on Silicon. These mirrors can be easily moved using electrostatic force due to their small mass. Figure 2 shows an SEM view of a torsional mirror produced at the Montana Microfabrication Laboratory (MML) at Montana State University, Bozeman.

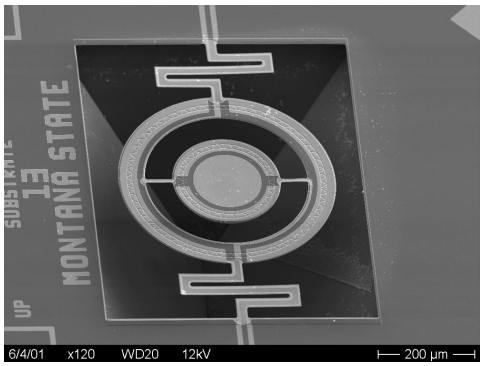


Figure 2. A torsional mirror produced at MML using the above described fabrication technology.

This paper presents a novel off-chip interconnect based upon a miniature coax that transitions to a Silicon microstrip transmission line to enable high speed signaling through SSN reduction. The transition will use MEMs process technology to form a plated trench that will accept a coaxial transmission line.

## III. Methodology

Micro-ElectroMechanical (MEM) fabrication technology has advanced in recent years to produce commercially available products used in the automotive and biomedical fields. The ability to reliably form mechanical features on an IC substrate has created an opportunity to apply novel approaches to the off-chip interconnect problem. Using micro-scale CMOS processes to form MEMs features enables a new approach to increasing the throughput of SoP systems.

MEMs technology can be adapted to form an off-chip coaxial to microstrip launch for the transport of high-speed digital signals. In this approach, a trench is etched into the IC substrate and then plated with a conducting material. This forms a ground connection for a mini-coaxial conductor whose center conductor extends out of the shield. This mini-coaxial conductor can be laid into the trench such that the outer shield of the coax contacts to the plated trench on the IC substrate forming a connection between the coax and the IC substrate ground. The center conductor of the coax is similarly laid onto an exposed outer layer microstrip trace on the IC substrate forming the signal path. This approach would yield a coaxial launch to transmit signals on and off the IC using a shielded conductor. Figure 3 shows the approach.

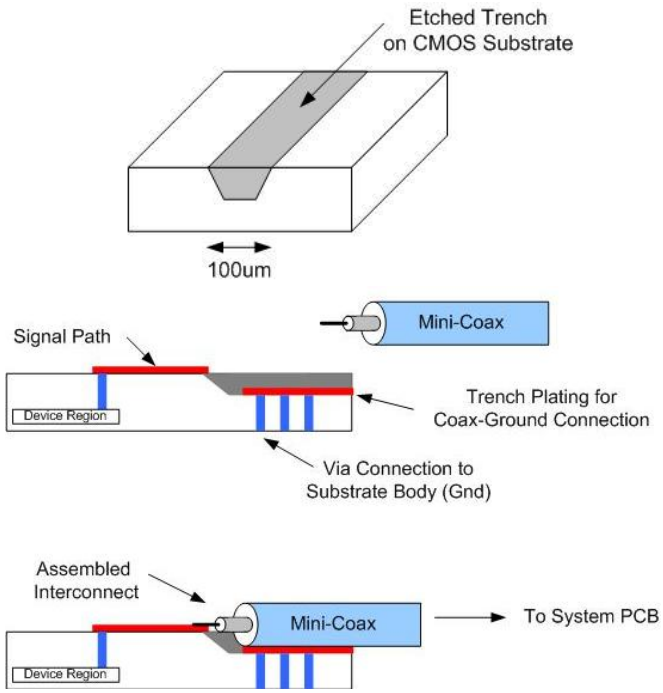


Figure 3. Off-chip coaxial to microstrip launch using MEMs trench.

This approach has inherent advantages. The first is that the shielding of the coaxial conductor eliminates any coupling within the package interconnect. The second is that size of the interconnect can be miniaturized relative to existing interconnect technologies. One of the reasons that modern interconnect is large relative to on-chip feature sizes is the mechanical assembly processes that are used. The machines that handle the interconnect have limited accuracy so the feature sizes must be large enough to overcome this error. The MEMs trench in this approach has inherent alignment features that reduce the error of robotic assembly. When the mini-coax is placed into the trench, a downward vertical force can be applied to the coax and the trench will automatically align the center conductor to the microstrip trace on the IC as the coax slides downward. With this alignment issue addressed, the physical size of the interconnect can be reduced which leads to increased electrical performance.

## IV. Feasibility Study

The first step in examining the feasibility of this approach is to examine the spatial considerations of such a design. Then the electrical parameters can be compared between the new interconnect and existing off-chip interconnect to evaluate the improvements.

### *A. Coaxial Transmission Lines*

A coaxial line is a controlled impedance transmission line in which the signal travels on a center conductor and the return current travels on an outer shield sharing the same axis. The dimensions of the two conductors, in addition to the dielectric material between them dictates the impedance and propagation constant of the transmission line. In this application, the inner conductor of the coax line must be accessed in order to make contact to the IC substrate conductor. To accomplish this, the outer shield is recessed exposing the center conductor and the dielectric. This allows the center conductor to extend out of the coax shield but still have a distance where it is covered with dielectric to avoid inadvertent shorts to the outer shield. Once the center conductor and the dielectric are securely out of the outer shield, the dielectric can then be removed leaving only the center conductor. The following figures show the coaxial dimensions and the recession of coaxial components in order to expose the center conductor.

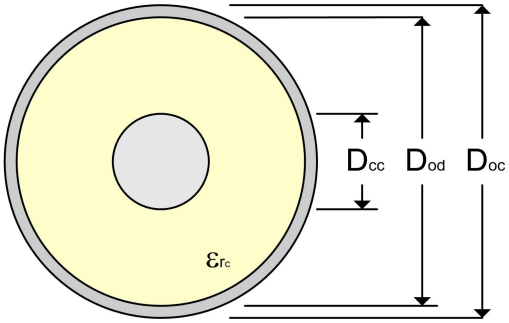


Figure 4. Dimensions of a coaxial transmission line.

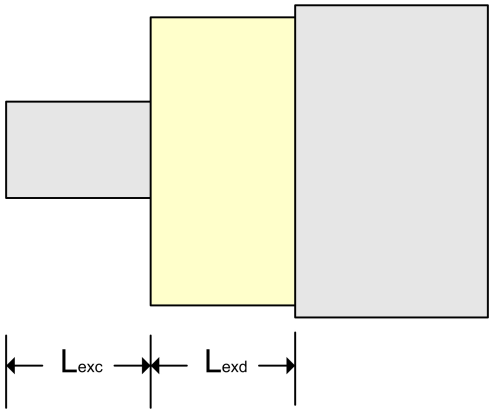


Figure 5. Dimensions of the coaxial transmission line recession of outer shield and dielectric in order to expose the center conductor.

When a wave is traveling within the coaxial structure, the impedance is given by [18]:

$$Z_{0_{coax}} = \frac{138}{\varepsilon_r} \cdot \log\left(\frac{D_{od}}{D_{cc}}\right) \quad (1)$$

As the signal transitions out of the coaxial region, it will undergo a change in impedance that can no longer use the closed solution given in equation 1.

*B. Microstrip Transmission Line*

A microstrip line is a controlled impedance transmission line in which the signal travels on a rectangular trace above an infinite ground plane. The dimensions of the rectangular conductors, its position relative to the ground plane, and the dielectric material used dictates the impedance and propagation constant of the transmission line. In this application, the rectangular conductor is implemented on a Silicon substrate using an outer metal layer. The ground plane is implemented using an inner metal layer. The outer layer conductor will attach to the exposed center conductor of the coaxial transmission line. The following figure shows the dimension of a microstrip transmission line.

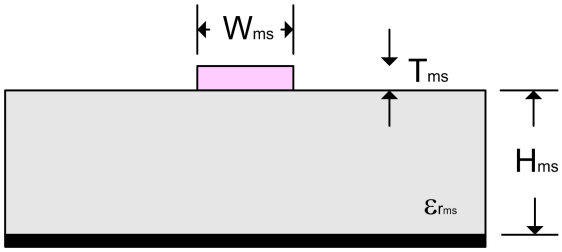


Figure 6. Dimensions of a microstrip transmission line.

When a wave is traveling within the microstrip structure, the impedance and effective dielectric constant are given by [18]:

$$Z_{0_{ms}} = \frac{120 \cdot \pi}{\sqrt{\varepsilon_{eff}} \cdot \left[\frac{W_{ms}}{H_{ms}} + 1.393 + \frac{2}{3} \cdot \ln\left(\frac{W_{ms}}{H_{ms}} + 1.444\right)\right]} \quad (2)$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2 \cdot \sqrt{1 + 12 \cdot \left(\frac{H_{ms}}{W_{ms}}\right)}} \quad (3)$$

*C. MEMs Trench*

In order to mechanically align and support the coaxial to microstrip transition, a polygonal shaped trench is etched into the Silicon substrate. This trench is plated and makes electrical contact with the outer shield of the coaxial transmission line. Figures 7 and 8 show the dimensional parameters of the trench.

*D. Impedance Boundaries*

The construction of this launch creates regions of different characteristic impedance. Characteristic impedance is the relationship of voltage to current in a transmission line and can be defined in terms of the per unit inductance and capacitance [18]. The capacitance and inductance at any point along the transmission line is dependant upon the geometric structures that carry the signal and the return path. Figure 9 shows the cross sections of different regions within this launch that have different impedance characteristics.

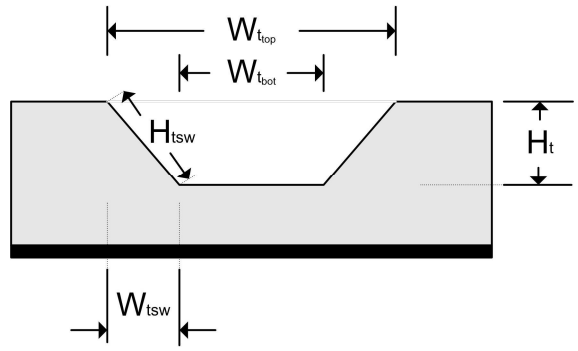


Figure 7. Dimensions of the MEMs trench that will facilitate the coaxial to microstrip transition.

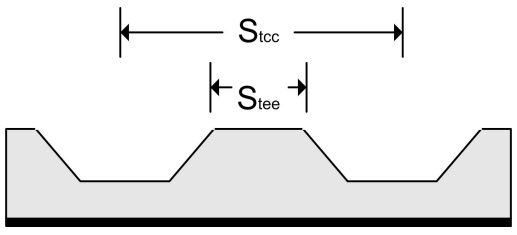


Figure 8. Spacing between multiple adjacent trenches on a single substrate.

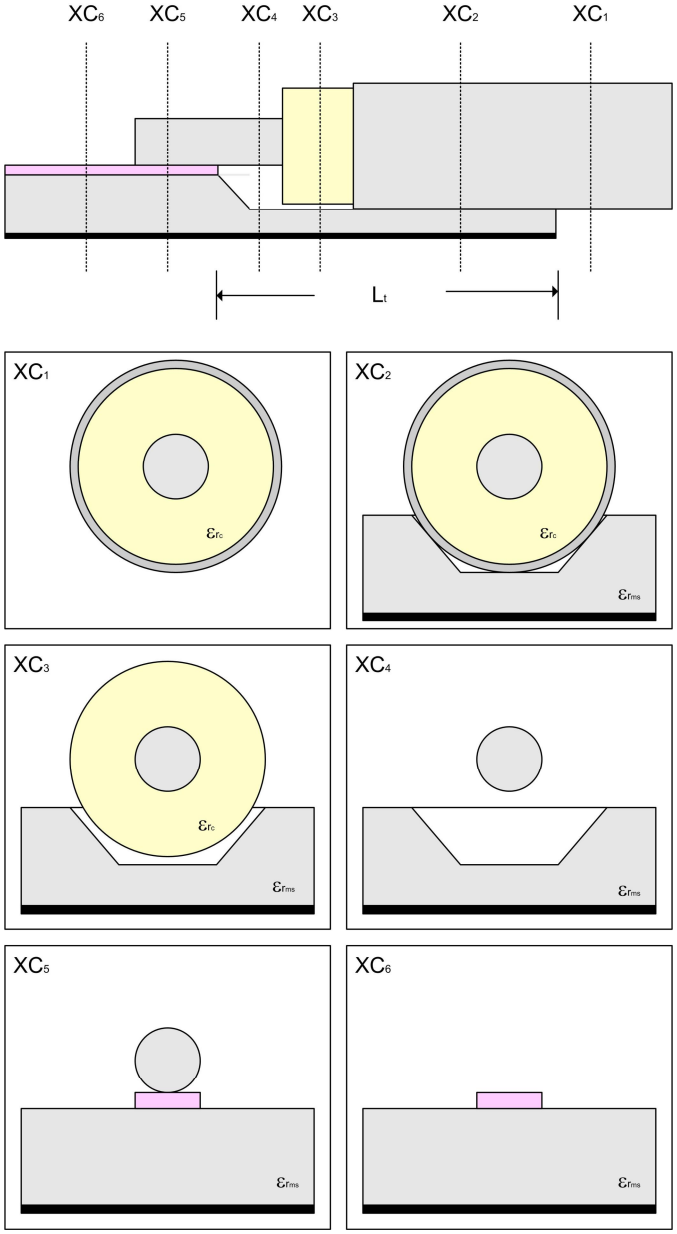


Figure 9. Cross sections of the coaxial to microstrip launch.

The cross sections $XC_1$ and $XC_6$ have closed-form solutions for the characteristic impedances, propagation velocity, and can be approximated using a variety of methods. In addition, both of these transmission line structures have been studied extensively and the coupling and SSN components are well understood. Cross-sections $XC_2$ through $XC_5$ are regions that are created due to the construction and assembly processes used to attach the off-chip coaxial line to the Silicon substrate. These regions will have difference impedances depending on the geometries that carry the signal and return current. These structures can be analyzed independently and closed-form solutions can be found to describe the impedance. However, this type of analysis is ideal for finite element analysis in which the electromagnetic fields can be modeled as they propagate from the coaxial region to the microstrip.

*E. Spatial Dependencies*

The first step in evaluating this type of interconnect is to define the interdependencies between the geometries. The key dimension that will drive the rest of the structures' construction will be the diameter of the coaxial center conductor (Dcc). This dimension will be dictated by the geometries of commercially available wire that are suitable for this application. Another constraint on the wire diameter that limits how thin it can be is the ability to create a coaxial line from it. Currently, wire gauges (AWG) of 42 through 50 meet the spatial needs of this application. From this dimension, the outer diameter of the coaxial dielectric ($D_{od}$) can be calculated using equation 1. Coaxial cables have recently been introduced commercially using 42AWG wire to produce 50Ω transmission lines [19,20]. The outer shields of thin wire coaxial lines ($D_{oc}$-$D_{od}$) are typically implemented by wrapping a metallic foil around the center wire which has been encapsulated in a thermally extruded dielectric material. The thin foil is typically a fraction (0.1 to 0.5) of the thickness of the center conductor diameter for thin wires [19,20]. This thickness is added to $D_{od}$ to define $D_{oc}$. For this work, we assume that the outer shield is $0.25 \cdot D_{cc}$.

The trench dimensions are defined following an octagonal shape. $W_{tbot}$ is one of the sides of the octagon assuming that the coaxial outer circumference is inscribed within a perfect octagon. This allows the bottom width of the trench to be described as:

$$W_{t_{bot}} = D_{oc} \cdot \tan(22.5) \tag{4}$$

The center point of the coaxial signal conductor will reside above the bottom of the trench $D_{oc}/2$. The top of the trench needs to be beneath the center point of the coax enough to accommodate the radius of the center conductor in addition to the thickness of the microstrip trace so that when the coaxial line is laid in the trench the center conductor makes perfect contact with the on-chip trace. This allows the vertical height of the trench to be written as:

$$H_t = \left(\frac{D_{oc}}{2}\right) - \left(\frac{D_{cc}}{2}\right) - T_{ms} \tag{5}$$

This dimension can then be used to describe the other key dimensions of the trench structure as:

$$H_{tsw} = \frac{H_t}{\sin(45)} \tag{6}$$

$$W_{tsw} = \frac{H_t}{\tan(45)} \tag{7}$$

$$W_{t_{top}} = W_{t_{bot}} + 2 \cdot W_{tsw} \tag{8}$$

The dimensions for the trench will influence the DRIE and release processes during fabrication. The dimensions for the coaxial conductor extension and corresponding trench ($L_{exd}$, $L_{exc}$, $L_t$) will depend on the mechanical stability needed in order to reliably hold the coaxial line in place without putting excessive force on the microstrip trace. The final values for these dimensions will be determined through empirical experimentation. As a starting point, it will be assumed that the area for the launch will extend into the Silicon substrate as much as a typical wire bond pad. This dimension is typically 100 μm for a standard gold ball bond [21]. For this work, we will assume that $L_{exc}=L_{exd}=W_{tsw}$. We will also assume that $L_t=100\mu m$.

### *F. Electrical Parameters*

In order to understand if the coaxial to microstrip launch can improve electrical performance, the parasitic capacitance and inductance are calculated and compared to standard package interconnect types. In the proposed launch, the majority of the interconnect length resides in the coaxial portion of the line. We will compare the coaxial portion of the interconnect to a traditional wire bond and to a flip-chip interconnect. These are the most common types of interconnect for connecting an IC substrate to a package.

For this case, the wire bond used is a 25 μm diameter, gold wire which forms a ball bond on the Silicon and package substrates using 100μm x 100μm pads [22]. The flip chip bump used has an average diameter of 125 μm and an average collapsed height of 75 μm using 100μm x 100μm pads [22].

Table 1 lists the parasitics for each type of interconnect. The coaxial line is listed for 3 different center conductor wire gauges (42, 46, and 50 AWG) using an inner dielectric constant of $\varepsilon r=2.1$ [19,20]. The microstrip dielectric is $\varepsilon r=4.5$.

| Par | Units | Wire Bond | Flip Chip | Coaxial Line | | |
|---|---|---|---|---|---|---|
| | | | | $42_{AWG}$ | $46_{AWG}$ | $50_{AWG}$ |
| $D_{CC}$ | μm | - | - | 64 | 41 | 25 |
| $D_{OD}$ | μm | - | - | 214 | 137 | 84 |
| $D_{OC}$ | μm | - | - | 230 | 147 | 90 |
| $T_{ms}$ | μm | - | - | 10 | 10 | 10 |
| $W_{ms}$ | μm | - | - | 64 | 41 | 25 |
| $H_{ms}$ | μm | - | - | 41 | 29 | 20 |
| $W_{tbot}$ | μm | - | - | 95 | 61 | 37 |
| $H_t$ | μm | - | - | 73 | 43 | 23 |
| $H_{tsw}$ | μm | - | - | 103 | 61 | 32 |
| $W_{tsw}$ | μm | - | - | 73 | 43 | 23 |
| $W_{ttop}$ | μm | - | - | 241 | 147 | 83 |
| L' | nH/m | 569 | 65 | 242 | 242 | 242 |
| C' | pF/m | 26 | 8 | 97 | 97 | 97 |
| Zo | Ω | 148 | 91 | 50 | 50 | 50 |
| $L_{5mm}$ | nH | 2.85 | 0.32 | 1.21 | 1.21 | 1.21 |
| $C_{5mm}$ | pF | 0.13 | 0.04 | 0.48 | 0.48 | 0.48 |

Table 1. Electrical parameters comparing the coaxial line interconnect to a wire bond and a flip-chip bump.

This table illustrates that by moving to the coaxial off-chip interconnect, the wire bond parasitic inductance can be reduced by 57% and the parasitic capacitance by 73%. In addition, the impedance of the coaxial line can be controlled to yield a standard 50Ω transmission line versus the uncontrolled 148Ω impedance of the wire bond. The coaxial line has more parasitic inductance and capacitance than the flip-chip bump, however the impedance has been reduced by 41Ω to yield a controlled 50Ω transmission line. The area required for the 42 AWG and 46 AWG coaxial line transition ($W_{ttop}$) is larger than the 100 $\mu m^2$ pads used for the standard interconnect. However, the 50 AWG coaxial launch takes 17% less area.

These results illustrate that the coaxial to microstrip launch has potentially significant electrical and spatial advantages over standard off-chip interconnect technology currently being used and is worth further investigation.

## V. Future Work

The next step in understanding this novel interconnect is to perform finite element analysis (FEA) simulations to evaluate the impedance mismatches and radiation patterns due to the coaxial to microstrip transition. Figure 10 shows the initial 3D model for this interconnect constructed in the *Ansys* FEA simulation tool.

In addition, prototypes of this interconnect are currently being investigated at the Montana Microfabrication Laboratory at Montana State University, Bozeman. This facility has the experience with DREI used to build MEMs trenches. Initially, commercially available 42 AWG, 50Ω coax cables [19,20] will be used to prove the feasibility of assembling this launch. Experimentation into creating 46 AWG and 50AWG coaxial lines using oxide growth and metal plating will be performed at MML to create micro scale coax lines.

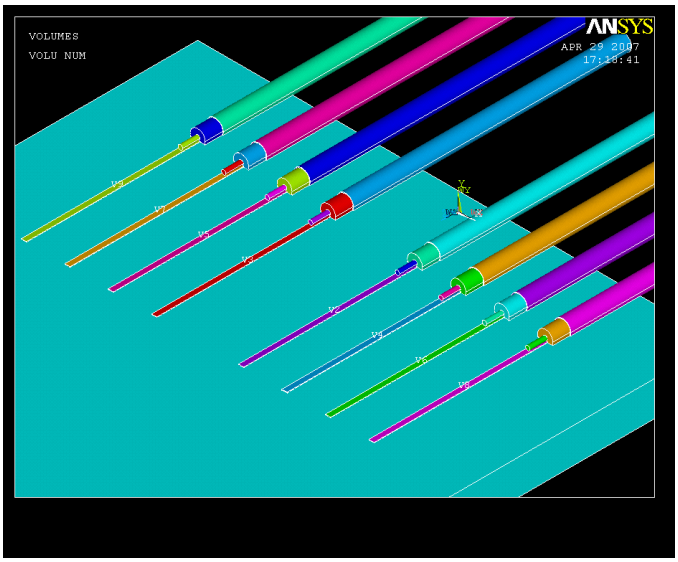


Figure 10. 3D FEA Model of coaxial to microstrip launch.

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