Differential Logic Analyzer Probing

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Over the past decade, digital signal speeds have increased at an exponential rate. This performance increase has brought signal integrity to the forefront of technology in the engineering community. Microwave design methodologies that once were only applied in high-end applications are now used in most every mainstream digital design. To meet the demand of future data rates, engineers are turning to advanced signaling methodologies. One that is starting to be used widely in industry is differential signaling. In order to assist design engineers as they begin to implement systems based on differential signaling, the test and measurement community is now offering a large suite of validation equipment based on differential measurements. Mainstream test equipment such as logic analyzers, oscilloscopes, and network analyzers are all providing differential measurement capability.

Fundamentals of Differential Signaling

Differential signaling has many inherent advantages over traditional single-ended systems. The basic definition of differential signaling is that two lines are driven from the transmitter to the receiver, one sending the "True" value of the signal and the other sending the "Complement." The receiver compares the two signals to determine the logic level intended (ie, A - B). This methodology is beginning to be adopted in digital system designs as one method to overcome signal integrity problems. The three main inherent advantages of differential signaling are signal-swing doubling, common-mode rejection, and return current provision.

Differential Logic Analyzer Probing

A logic analyzer is a powerful tool when debugging and validating a digital system. As digital transport systems are moving toward differential signaling, logic analyzer vendors are providing differential probes to assist in the development of these systems. Just as it is important to understand differential signaling basics for the success of the system, it is also important to understand the differential logic analyzer probe to ensure the success of the measurement.

The Logic Analyzer As A Differential Receiver

The first thing to consider is that the probe acts as a differential receiver. This means that it will perform the A - B operation just like the target receiver. It is prone to all of the same design issues that are present on the target. In an ideal measurement, the probe should observe the same signal as the differential receiver. Specifically, any common-mode noise on the pair, or phase difference between the pair should be the same at the probe tip as it is at the receiver. This ensures that the measurement taken accurately reflects what is truly happening in the differential system.

Probe Location

A second consideration is probe location. Noise that is common-mode to the receiver may appear as differential noise to the logic analyzer probe due to probe location. Take for example the routing diagram of a loosely-coupled differential pair in Fig. 1.

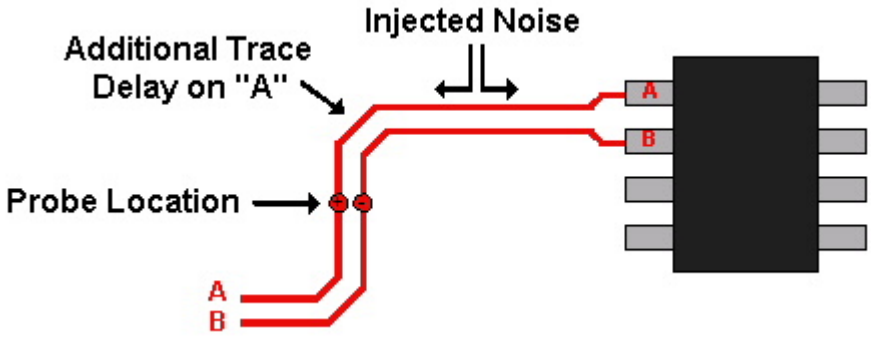


Fig. 1: Probe Location Of A Differential Measurement

Noise is injected on both lines of the differential pair close to the receiver. The receiver observes the forward traveling noise on both A and B and rejects it when performing the logic decision (A - B). Now consider the reverse traveling noise as it appears at the probe tip. Due to a routing turn, the noise on the True side (A) is delayed with respect to the Complement side (B). This causes the noise to appear as two separate differential discontinuities that are not rejected by the analyzer. In this case, the logic analyzer observes a signal that is not representative of what the target receiver sees. The solution to this is to probe the system where common-mode noise is not observed as differential noise. The best place to probe would be directly at pins of the receiver. This is the location that will best represent what the differential receiver circuit on the target is seeing.

Common-Mode Input Range

A third consideration to account for is the common-mode input range (CMIR) of the probe. Differential receivers traditionally use a common-mode to differential topology. A logic analyzer probe is comprised of two single-ended amplifiers (Fig. 2), both referenced to ground. One amplifier receives the True side and the other receives the Complement. The outputs of these two amplifiers are then fed to a differential amplifier that then performs the difference (A - B). This is done because there are limitations in implementing a fully-differential receiver. Standard differential receivers also follow this methodology.

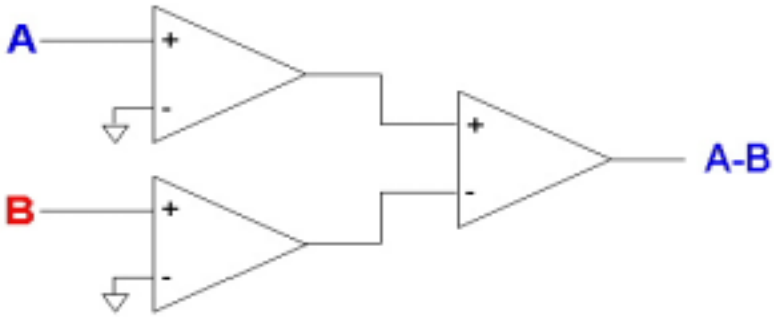


Fig. 2: Single-Ended to Differential Architecture

This is important to understand because the CMIR of the probe must be considered. In a fully-differential architecture, the probe would not be able to distinguish between a 1-V signal swing centered at 0 V, or a 1-V signal swing centered at 100 V. The net results in each case would be $\Delta V = A - B = 2$ V. However, in the architecture of Fig. 2 the signal swing needs to be within the CMIR of the two single-ended receivers in order to be observed by the 2nd stage differential amplifier. The reason that this is brought up is because design consideration may have been made for the CMIR of the receivers in the system but not for the CMIR of the logic analyzer. To ensure successful logic analysis, the CMIR specification of the probe must be considered.

Consider a system in which the net voltage exceeds the CMIR of the receiver. Any voltage exceeding this range will be clipped. This is a problem when one side of the differential pair has common-mode noise that is clipped while the other side of the pair has noise that is NOT clipped. This results in noise that is not seen as common-mode by the differential probe and thus not rejected.

Take the following example:

> A differential probe has a common-mode input range (CMIR) of 0.3 V to 3.0 V. The input signals are 800 mVpp centered at 2.0 Vdc (standard PECL). Each side experiences a common-mode noise spike in the amount of 750 mV which pushes the net voltage of the Complement side of the pair out of the CMIR of the probe, and the signal is clipped. This results in a difference between the noise spikes on each line. When the probe performs A - B, the result is a differential discontinuity. Fig. 3 shows the waveforms for this example.

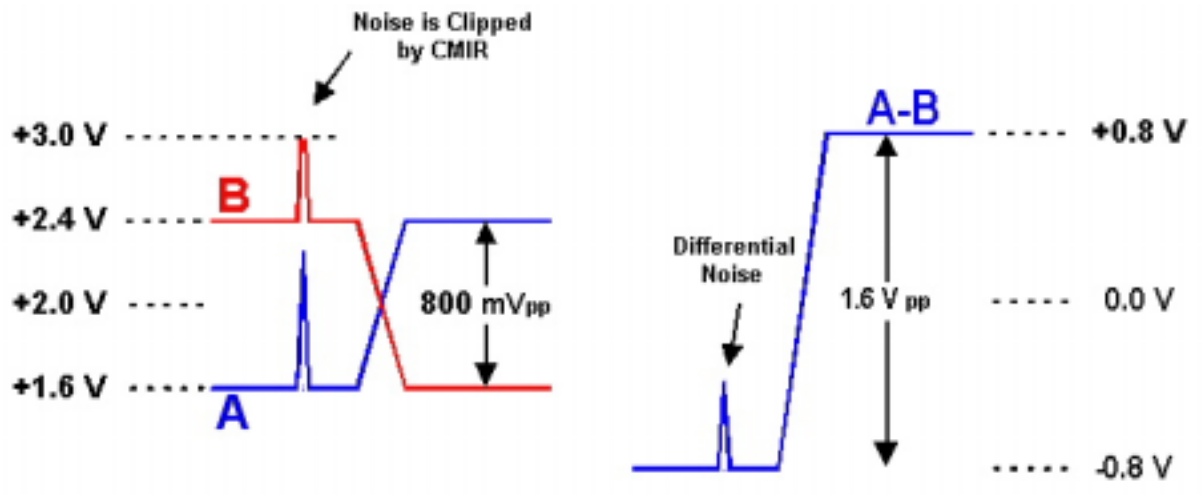


Fig. 3: CMIR Violation Resulting in Differential Noise

Common-Mode Component Removal

A final consideration in logic analyzer probing is that the common-mode component of the differential pair is not present in the final signal the analyzer sees. This means that when using signal integrity tools, such as *Eye Scan* by Agilent Technologies, the displayed analog signal will be centered at 0 V. This is because the common-mode component (or dc offset) has been removed during the differential operation A - B. The following figures show an example of this. The A and B analog inputs to the logic analyzer are observed by the *54845A Infiniium oscilloscope* in Fig. 4. Both signals are 400 mVpp with a dc offset of 1 Vdc. Fig. 5 shows the corresponding output of an *Eye Scan* measurement taken using the 16756A

logic analyzer. Notice that the *Eye Scan* measurement shows a resulting analog signal with an amplitude of 800 mVpp centered at 0 Vdc.

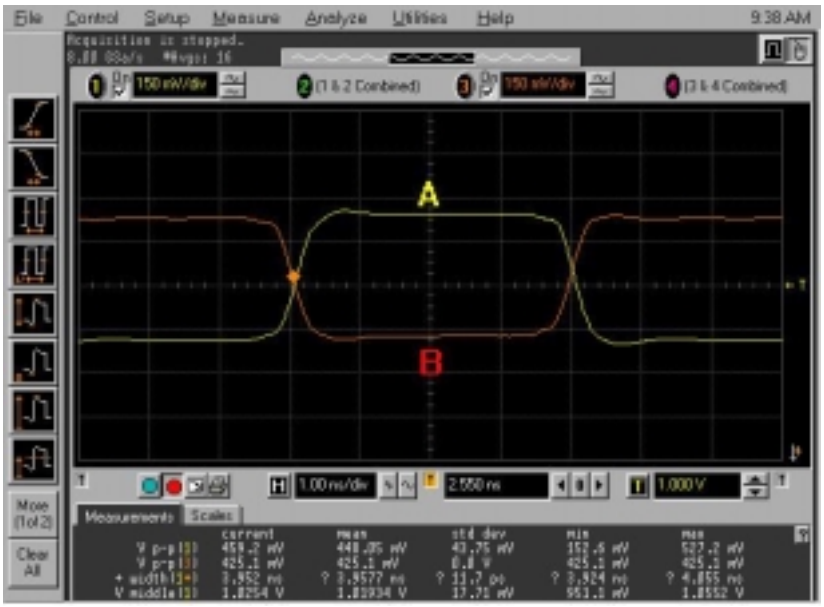


Fig. 4: Analog Inputs As Observed By The 54845A Infiniium Oscilloscope

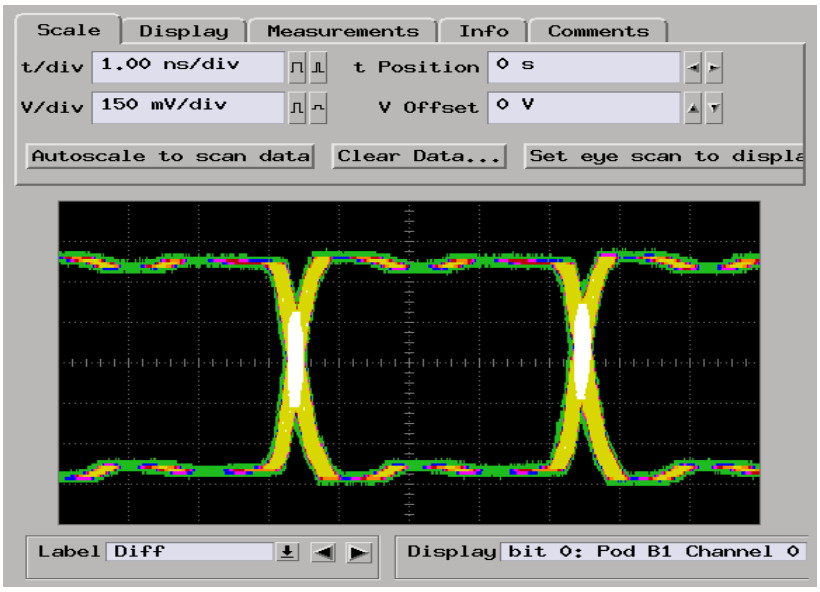


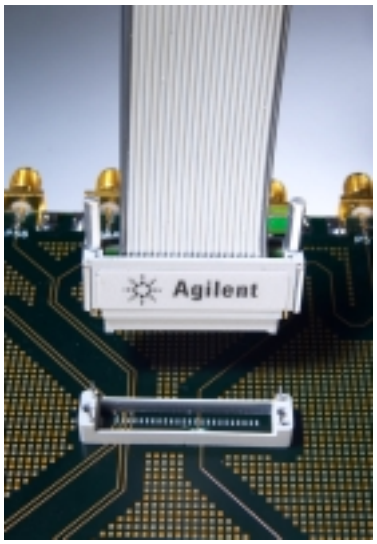
Fig. 5: *Eye Scan* Measurement From The 16756A Logic Analyzer

Modern Differential Logic Analyzer Probes

Logic analyzer probes come in three different form factors: flying lead, connector-based, and the new connector-less. The connector-based and connector-less probes are for the engineer that has designed-in testability on the PCB. The flying lead probes are traditionally for engineers who are observing signals that do not have designed-in test points. For all flavors of logic analyzer probes, differential solutions

exist. Fig. 6 shows examples of various differential probing form factors that are available today from Agilent Technologies.

Connector Based
(E5379A)



Connector-Less
(E5387A)

Flying Lead
(E5381A)

Fig. 6: Examples Of Modern Differential Logic Analyzer Probes

Conclusions

Differential signaling is being widely accepted as a methodology for negating many signal-integrity problems. As digital systems move towards differential signaling, logic analyzer vendors are providing differential probes to aid in the validation of these systems. It is important to note that the signaling fundamentals that are used to design successful high-speed differential systems are the same fundamentals that must be considered to provide successful differential measurements. By understanding and applying these fundamentals in the early stages of the design, successful logic analyzer testability can be used to ensure a robust digital system and decrease time to market.

About The Author

Brock LaMeres earned his BSEE from Montana State University and his MSEE from the University of Colorado. He is currently a hardware engineer for Agilent Technologies, where he designs high-speed printed circuit boards used in logic analyzers. Brock is also a part-time instructor in microprocessor systems at the University of Colorado in Colorado Springs. His research interests include modeling and characterization of transport systems and high-speed digital design.

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