When to make the move to advanced probing technology in logic analysis

By Brock J. LaMeres

Logic analyzers are the tool of choice for digital system engineers when debugging and validating their complex systems. As data rates increase, the physical probing connection can lead to signal integrity issues that prevent engineers from exploiting the full debug potential of the logic analyzer. The electrical load of the probe as well as the coupling within the probe will negatively affect the signals being observed. The probe can degrade the performance of the target signal to the point at which it fails solely due to the probe. In addition, the load of the probe can distort the target signal so that the signal that the logic analyzer observes is not representative of the original signal. This leads to measurement error and wasted time during debug.

Much work has been done in the test and measurement community to decrease the electrical load of the probe while still achieving a sound mechanical connection. Over the past decade, the standard method to probe digital signals using a logic analyzer was to use a matched impedance connector MICTOR). This connector is sufficient for rise times of ~1 ns (600 Mb/s) and above. However, as rise times continue to shrink, the MICTOR-based probe presents an electrical load large enough to cause the bus to fail (Figure 1). The electrical load is as great as 3 pF with a signal-to-signal coupling capacitance on the order of 1 pF. For rise times of 1 ns, this can cause up to 30% coupling between signals due to the probe. Another drawback of the MICTOR probe is that when a logic analyzer is not physically connected, a mating connector still resides on the PCB. The connector is a large physical structure that adds loading and coupling when a probe is not even connected. The physical size of the connector is the reason for the limited performance of the MICTOR connector. This is because any stub length between the probe tip network and the target signal will degrade the performance of the logic analyzer and increase loading on the target. Thus, the physical size of the probing interconnect is inversely proportional to electrical performance.

To address the problems associated with the MICTOR connector, logic analyzer vendors have introduced connectorless probing technology. In this style of probing, only small surface-mount pads are placed on the target PCB. The probe tip contains compression interconnect in the form of soft-touch micro-spring pins that form the electrical connection to the pads. A mechanical structure called a retention module is hand soldered to the target PCB, which aligns and retains the spring-pins as they contact the pads on the target. This new technology allows the probe tip network to reside physically closer to the target signal by decoupling the mechanical and electrical connection. The reduced stub length between the probe tip network and the target signal translates into increased performance and reduced loading. Current soft-touch connectorless probes have loading on the order of 0.7 pF with coupling on the order of 0.07 pF between signals (Figure 2). In addition, this interconnect has been verified for buses up to 3.125 Gb/s. Another benefit of this technology is that when the probe is not connected, the pads on the board have minimal loading (~80 fF) and insignificant coupling.

Selecting the appropriate logic analyzer probe is an engineering decision that is based on performance vs. cost. The MICTOR connector is less expensive than the soft-touch connectorless technology. If the probing application does not need the speed and reduced loading of a soft touch probe, then the MICTOR is a cost-effective solution that will deliver reliable measurement results. However, if the system under test is pushing the limits of today's technology and requires the latest advances in logic analyzer probing, then the soft touch connectorless probe is the answer. RFD

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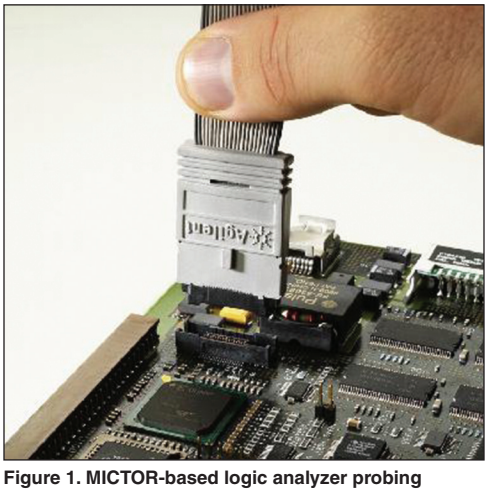

Figure 1. MICTOR-based logic analyzer probing presents an electrical load that can cause failures when data rates exceed 600 Mb/s.

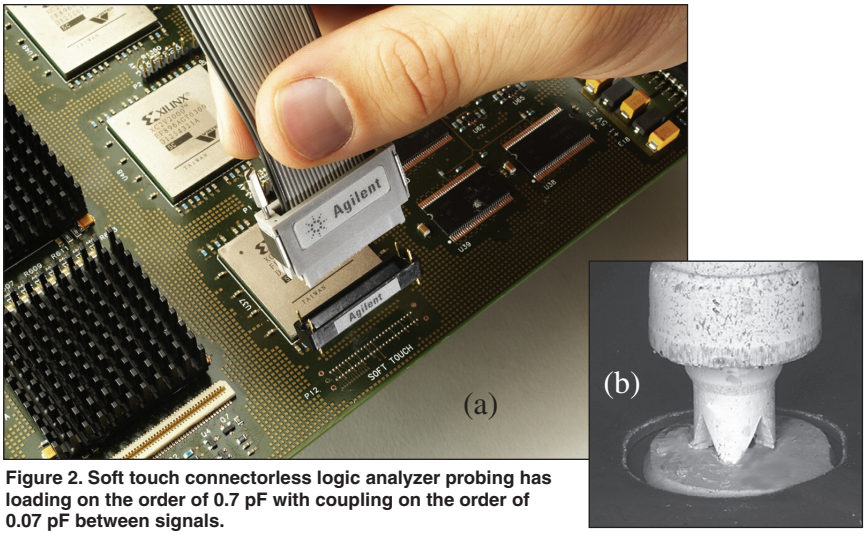

Figure 2. Soft touch connectorless logic analyzer probing has loading on the order of 0.7 pF with coupling on the order of 0.07 pF between signals.