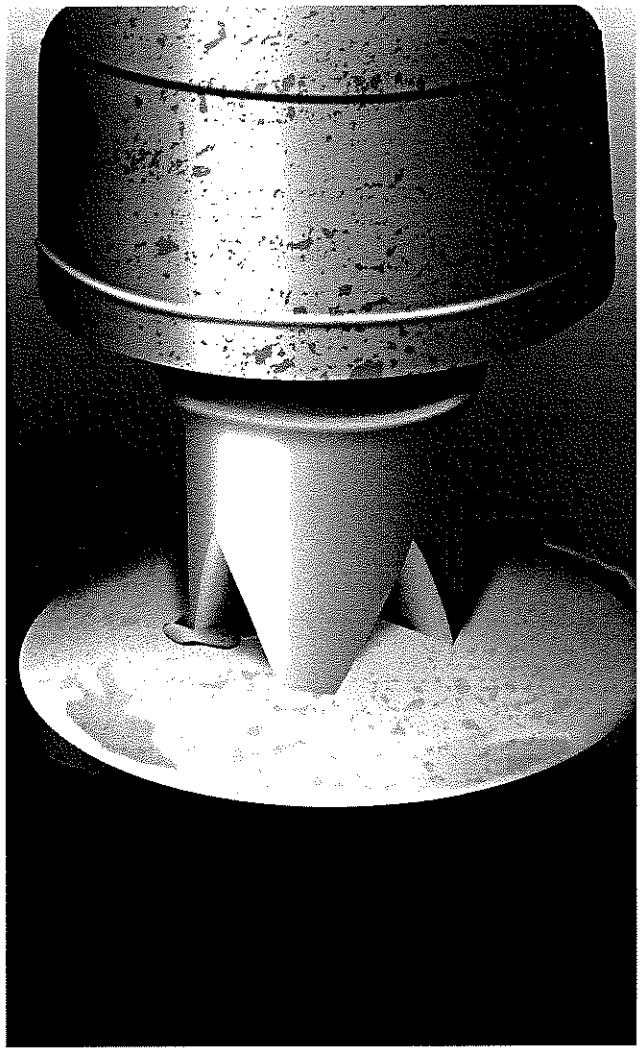
Compression probe technology makes sense in logic analyzers



Compression probe interconnect technology has mechanical and electrical advantages in logic analysis.

BY BROCK J. LAMERES AND BRENT A. HOLCOMBE

Logic analysis is a powerful tool in aiding engineers while debugging digital systems.

The physical connection between the logic analyzer and the target printed circuit board (PCB) is a major concern for engineers. The industry standard connection for logic analyzers over the past 10 years has been the Mictor connector. While this connector provides the high density connection desired, its electrical loading and mechanical reliability make it ill-suited for today's systems.

Compression-probe technology has emerged as the new industry standard to replace the Mictor connector. This new technology offers a host of electrical and mechanical advantages over the Mictor.

In compression-probe technology, the target system puts down surface-mount pads to which the signals of interest are routed. The logic analyzer probe has a compression interconnect that makes contacts with the SMT pads and forms the electrical connection. A separate mechanical retention module is placed on the target PCB that aligns and retains the compression interconnect onto the SMT pads.

This new methodology reduces the electrical loading on the target by reducing the physical structure of the interconnect. In addition, reliability is improved because the electrical and mechanical connections are decoupled.

Mechanical advantages

Connector-less probing offers a number of mechanical advantages over traditional connector-based probing. Connector-less probing involves turning the PCB into one half of the probing interconnect. This can essentially eliminate the need to include probing related components on the bill of materials for the PCB, greatly reducing the supply chain headaches that are typically associated with making the decision to include probing and debug capability early on in the design process.

With connector-less probing, the PCB designer needs only to place and route signals to a non-intrusive

> "Due to the major advantages of this new interconnect technology, it is finding broad acceptance in industry as the premier technology to probe digital buses."

footprint comprised of landing pads and small retention holes. When probing is required, a retention module (RM) is soldered down using a simple hand soldering iron found in most labs. Once the RM is soldered down, the connector-less probe can be attached and used to capture signals.

The non-intrusive nature of connector-less technology enables engineers to leave the footprint in a production design, which lets designers include probing capability at any point in the future after the product has been released. This helps reduce the cost associated with probing. For higher volume printed circuit boards, it is not cost effective to include even one extra connector on every board for probing. Now, with connector-less probing, designers are no longer forced to make a cost trade-off for debug. A product can ship with only the footprint on the board, which costs only the time to route signals to the pads. In the event that debug is needed in the field, all that is needed is to solder the RM onto the board and attach the probe.

Connector-based probes are limited by a maximum number of reliable mate and de-mate cycles. This limit is typically around 50 to 100 cycles. Connector-less probes can typically be used for thousands of cycles. Additionally, the compression interconnect on a connector-less probe has up to .025" of compliance, capable of absorbing the pad height variability of HASL finish. It also has the ability to pierce through oxides and contaminates on the pad, eliminating the need for cleaning of the surface to be probed (Fig. 1).

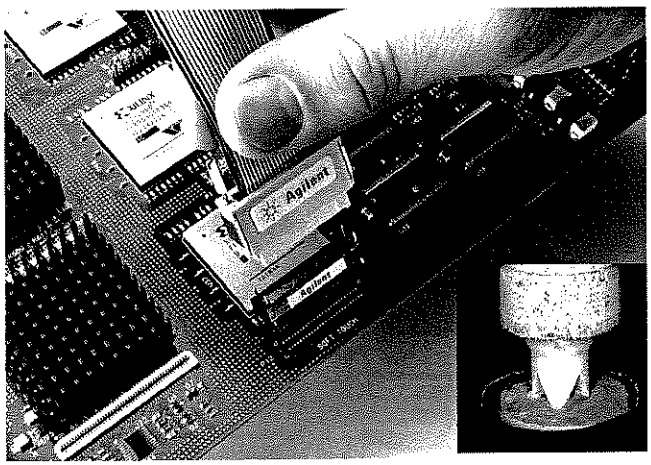


FIGURE 1. Connector-less probe technology with compression interconnects.

Electrical advantages

The goal of the probing connection is to present the least electrically intrusive load on the target system. Figure 2 (Page 16) shows the ideal probing scenario.

Loading is a term that refers to how much the original target signal is affected due to the probe. The goal is to make the probe's loading contribution small relative to the speeds at which the target system is running. The loading of a Mictor-based probe is 3 pF while the loading of a connector-less probe is only 0.7 pF. This difference is due to the reduction in the physical size of the probing interconnect, yielding greater than a 400% loading reduction when comparing connector-less to Mictor-based probing technology.

Another advantage of connector-less probing is the reduced loading of the footprint when the probe is not connected. In Mictor-based probes, a mating connector always resides on the target PCB. In most cases, unused traces connected to the connector are also on the board. The parasitics of the unused probe point are large enough that they cannot be ignored. Connector-less probe landing pads left on the board when the probe is disconnected produce little to no loading due to the pads (~80 fF).

In connector-less probing, only the landing pads are placed on the target PCB. These landing pads are spaced such that signals can be routed between the pads without changing signal layers. In Mictor-based probes, the connector that resides on the target PCB actually prohibits any routing through the

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connector due to its use of SMT and through-hole technology. This requires placing the connector off to the side, which has the disadvantage of increased loading due to the need for stub-traces.

With connector-less probing, the footprint can be placed directly in the signal path with minimal disturbance to the routing of the signals.

Connector-less applications

Many prominent applications are beginning to use connector-less probing when making the physical connection between the system and the debug equipment. Some of these solutions, detailed below, are HyperTransport, PCI Express, PCI Express Generation 2 and SRIO.

Additionally, general purpose connector-less probing is being adapted to enable digital designers to probe signals in a region where only a "low profile" or "right angle" egress of signals is possible.

Connector-less probing is new choice for acquiring data from the **HyperTransport bus.** Since the electrical interconnect and the mechanical retention are decoupled, this allows a much smaller electrical interconnect to be used. By doing this, the tip resistor of the probe circuit can reside physically closer to the target being probed. This reduces the electrical stub length between the target signal and the tip resistor, thus reducing parasitic loading on the target and improving the signal quality that the probe observes. Both of these factors lead to increased performance of the HyperTransport analysis probe.

When the **PCI Express bus** standard was developed in 2000, the industry adopted the first "midbus" style debug footprint to be used for digital debug using connector-less probing with a logic analyzer. This standard midbus footprint enables bus designers to route up to 16 serial "lanes" through the footprint to make these signals of interest available for debug using a logic analyzer.

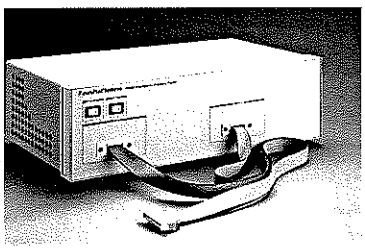

FIGURE 3. The HyperTransport probing solution using connector-less technology.

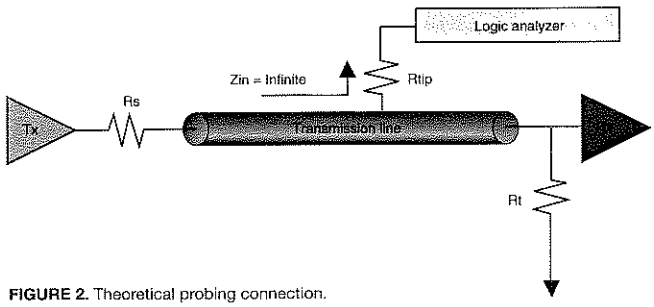

FIGURE 2. Theoretical probing connection.

This application of connector-less probing was in fact the first instantiation of connector-less probing in the industry. The unobtrusive mechanical space requirements and low electrical loading (<0.4 pF) on the target, made connector-less probing the ideal choice for capturing these signals, which can go as fast as 3.125 Gbits/sec.

In 2004, connector-less probing was once again chosen to implement **PCI Express Generation 2.** Using the same basic footprint and RM, connector-less technology will aid designers in being able to effectively capture signals up to 5.0 Gbits/sec without corrupting the bus' signal integrity.

Serial Rapid IO (SRIO) is an emerging serial bus architecture being used by network and telecom systems designers to build high-speed backplanes for connecting telecom equipment and computer servers to one another.

The SRIO bus is designed to run four serial lanes up to 3.125 Gbits/sec. As with PCI Express, SRIO has adopted connector-less probing as the standard for observing bus signals for system debug.

Probing for SRIO is implemented using the same 16- and 8-channel standard midbus footprints used for PCI Express. The probes being offered by logic analyzer vendors are also the same as the PCI Express 16-channel probe and the 8-channel "half size" probe.

Digital designs are becoming increasingly dense to the point that it has become necessary for probing solutions to be adapted to multiple form factors. One new adaptation of connector-less probing is the **"low profile" or "right angle"** connector-less probe. This new probing solution implements all of the electrical advantages of the standard "vertical" form factor connector-less probe (<0.7 pF loading, >2.5 Gbits/sec data rate), while adapting the mechanical form factor to reduce the overall height of the probe off the surface of the target to less than 0.265" tall when plugged in to the footprint.

A "right angle" connector-less probe finds many useful applications, such as with memory DIMM (Fig. 4).

Another application would be in the automotive debug world where it is often necessary to fit a probing solution into a stacked board design while evaluating the thermal and electrical impact on the device under test simultaneously (Fig. 5).

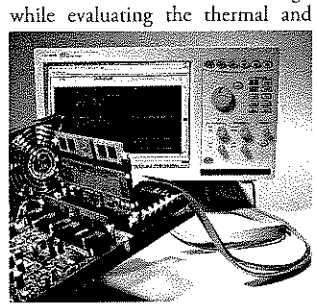

FIGURE 4. Low-profile connector-less probing technology is used in memory debug applications.

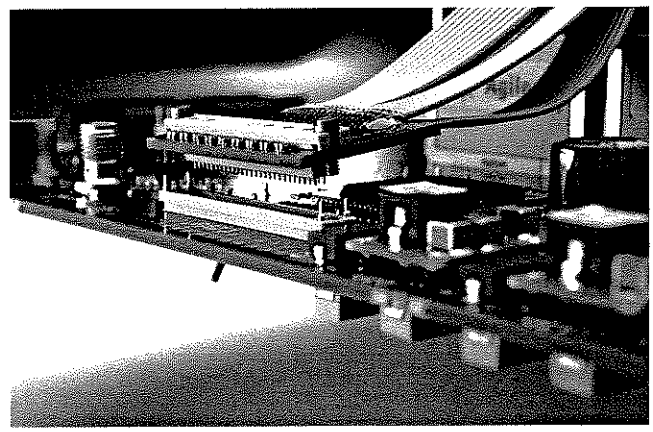

FIGURE 5. A low-profile connector-less probe.

Pushing the envelope

As digital data rates continue to increase, designers are migrating to connector-less probing technology and are reaping the benefits of a more reliable connection with minimal loading and simple to implement features on the target PCB.

This new technology and follow on proliferations for various applications are allowing designers to achieve successful logic analysis as they push their systems to higher data rates. **CS**

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